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MS-AC79

Ver: 0A

Intel -SugarBay plamform

CPU:

INTEL - Ivy/Sandy bridge LGA1155

System Chipset:

INTEL-Cougar Point

OnBoard Chipset:

HD Audio Codec:ALC887

LAN-RTL8111E

SIO:Fintek F171808A

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

MINIPCI Express (X1) Slot * 2

PWM:

Controller:NCP6131 3+1Phase

Other:

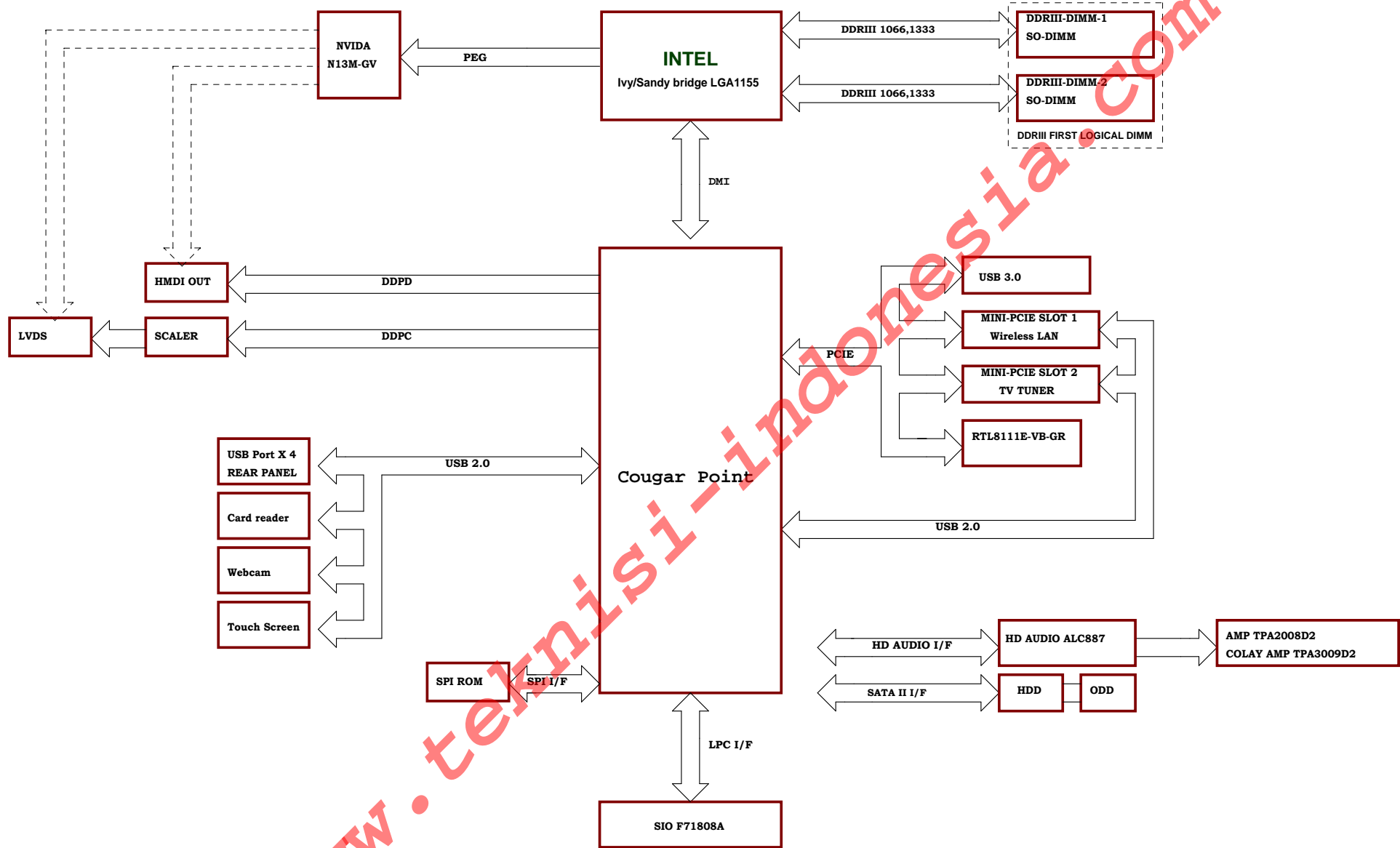
SATA(SATA2-300MB/s) *2

USB2.0 *4

USB3.0 *2

HDMI OUT*1

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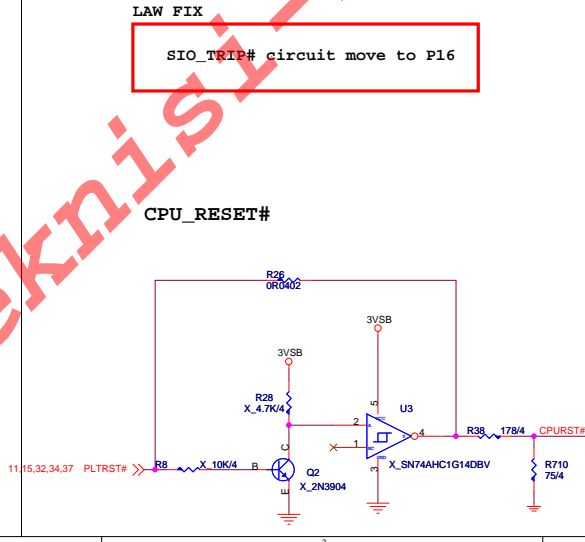
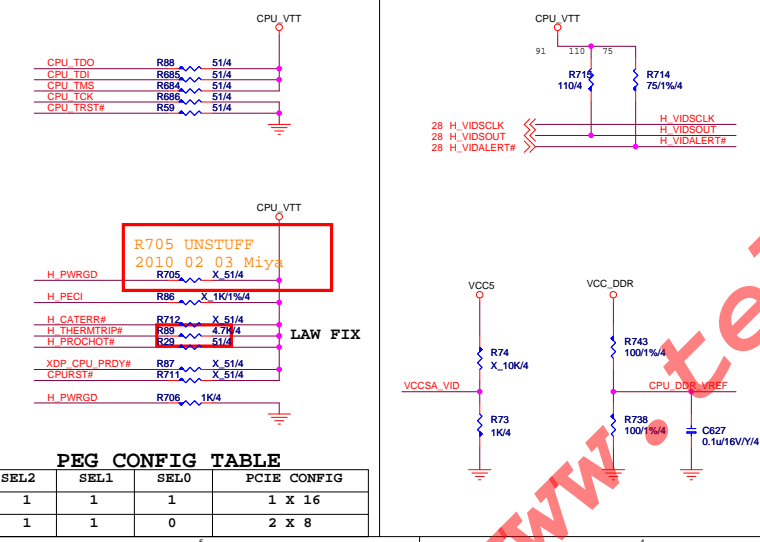
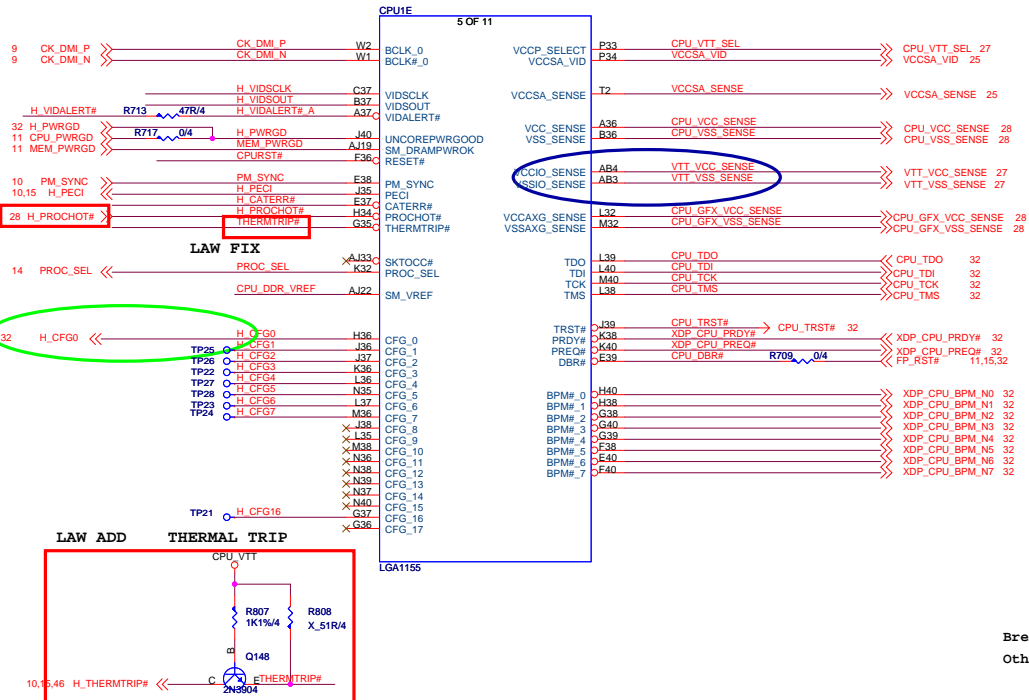


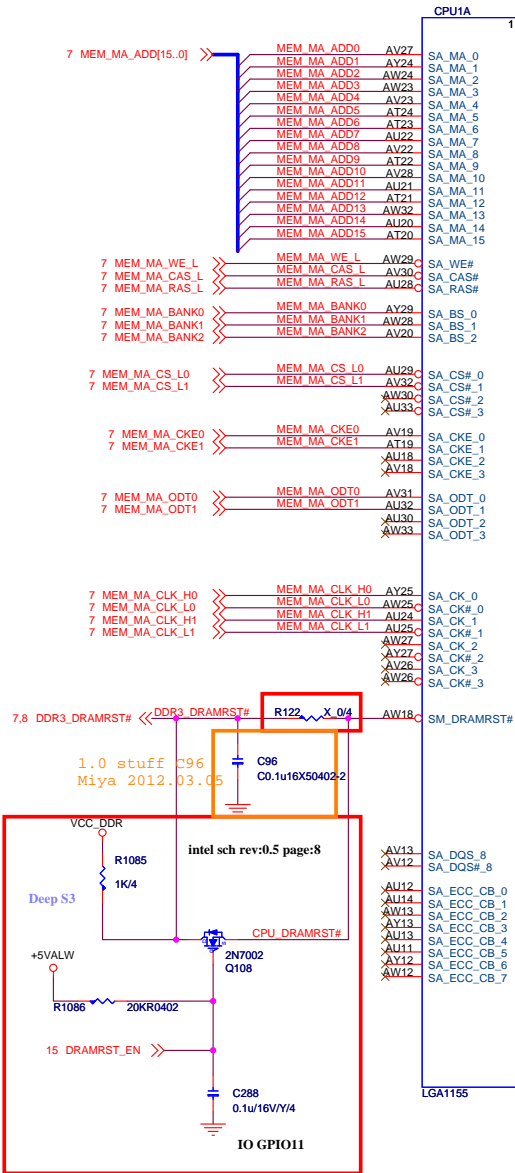
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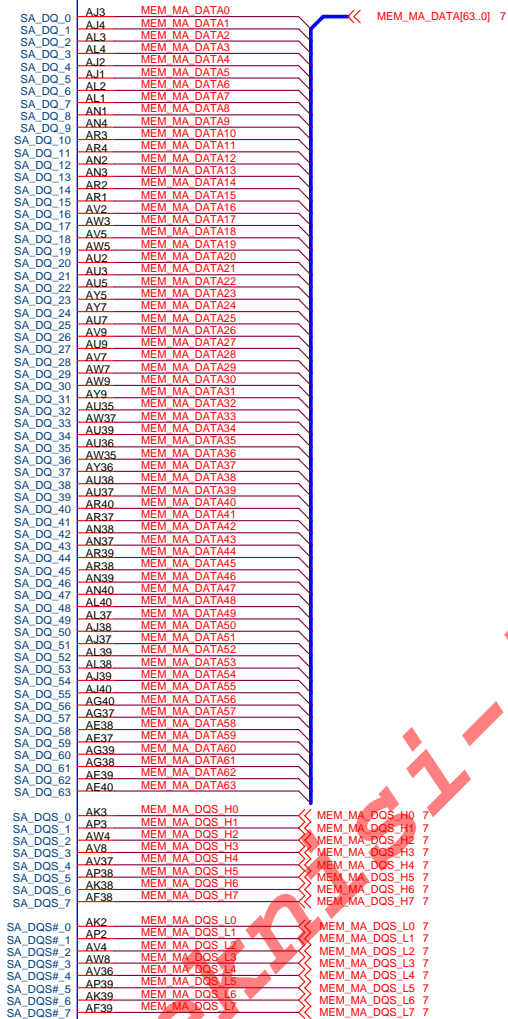
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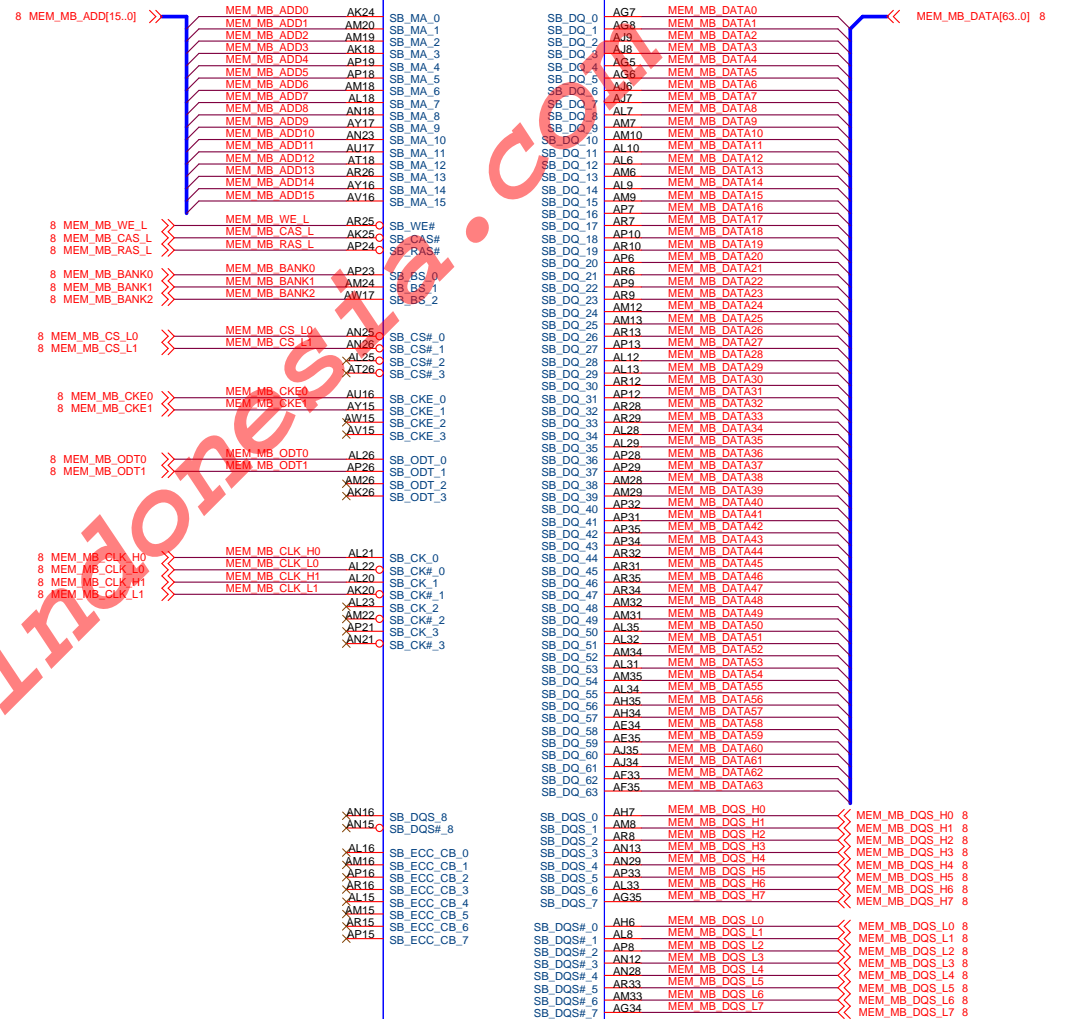


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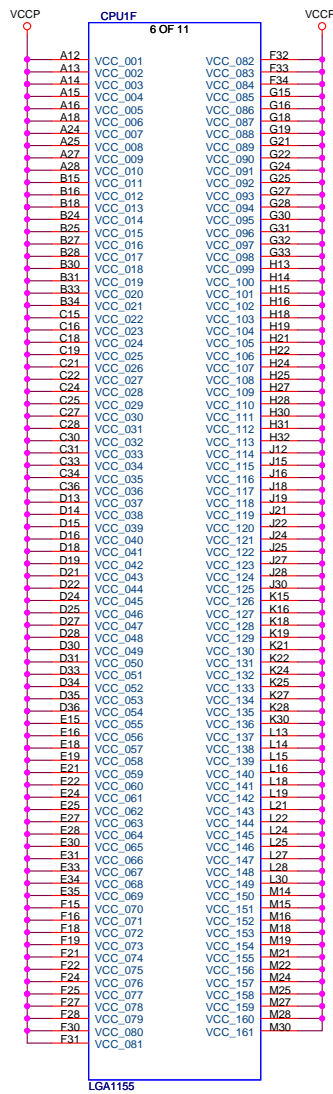
LGA1155



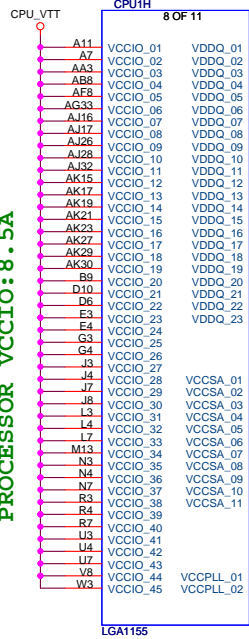
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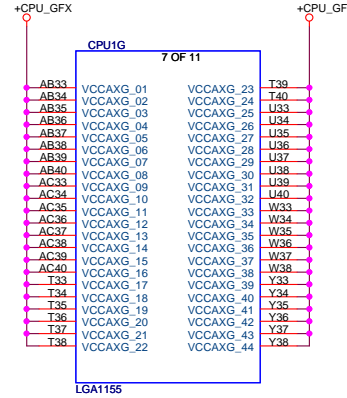


PROCESSOR VCCIO:8.5A



PROCESSOR VDDQ:4.75A

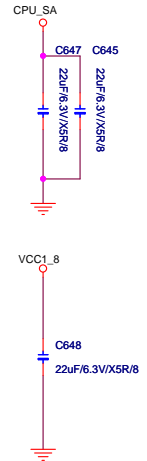
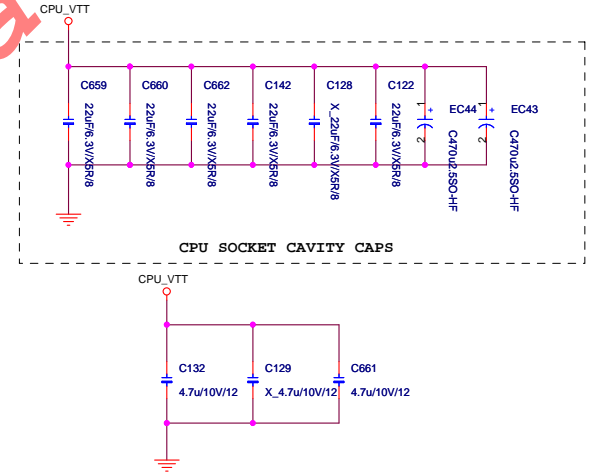
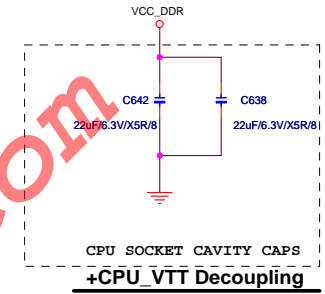
PROCESSOR VAXG:35A

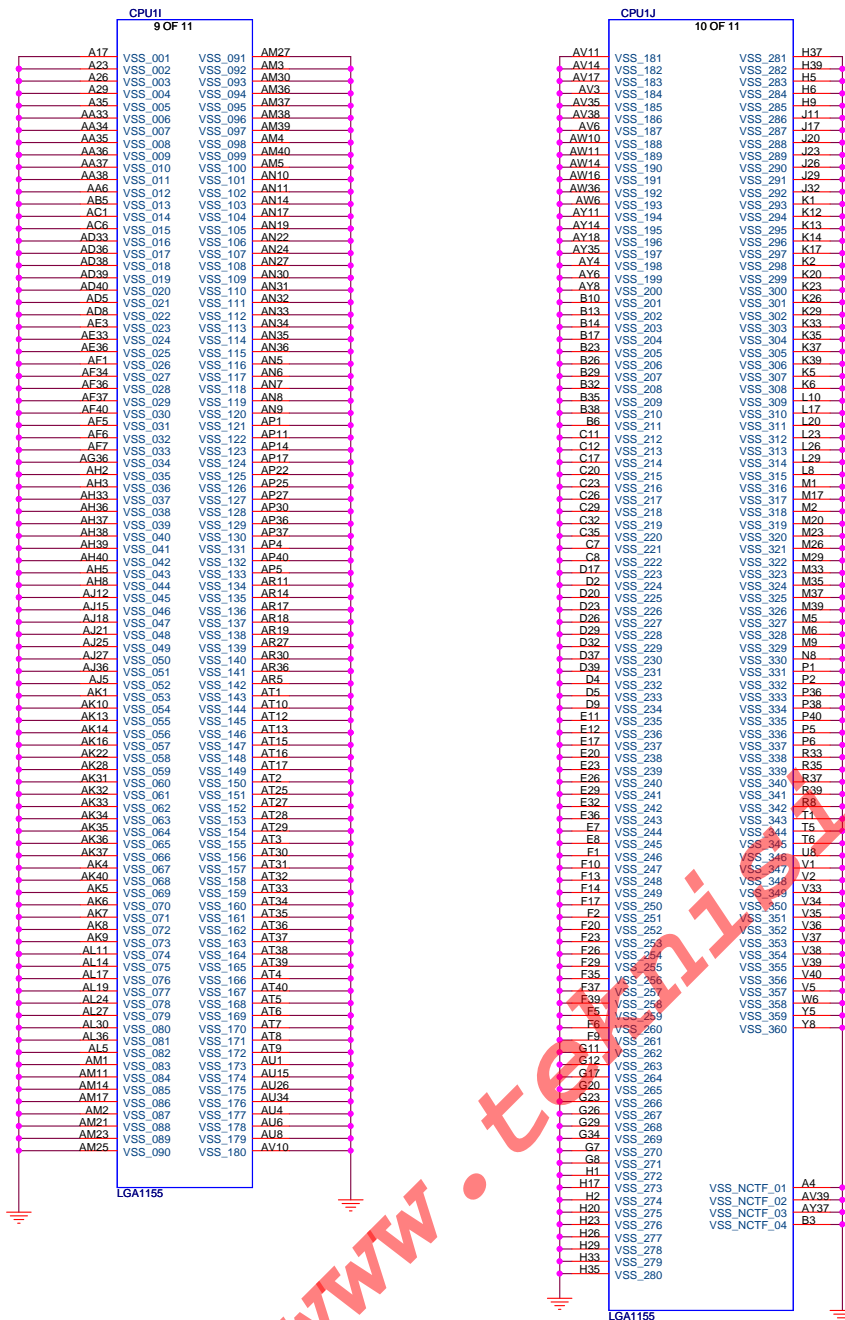


PROCESSOR VCCSA:8.8A

PROCESSOR VCCPLL:1.5A

+1.5V_DDR3-Decoupling





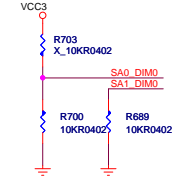
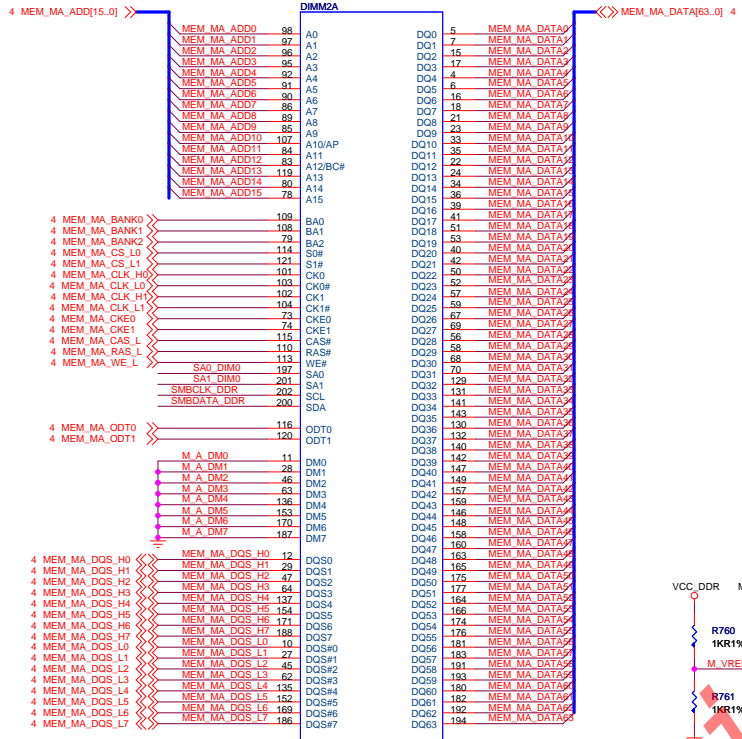
9.32 XDP_CPU_BCLK_P
9.32 XDP_CPU_BCLK_N

XDP_CPU_BCLK_P
XDP_CPU_BCLK_N

R707
R708

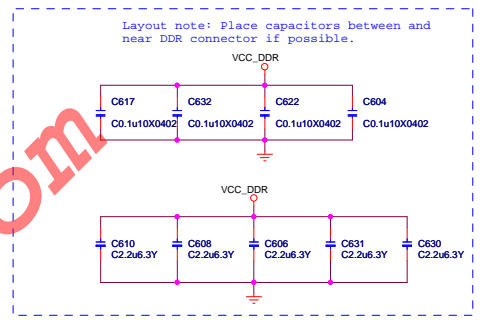
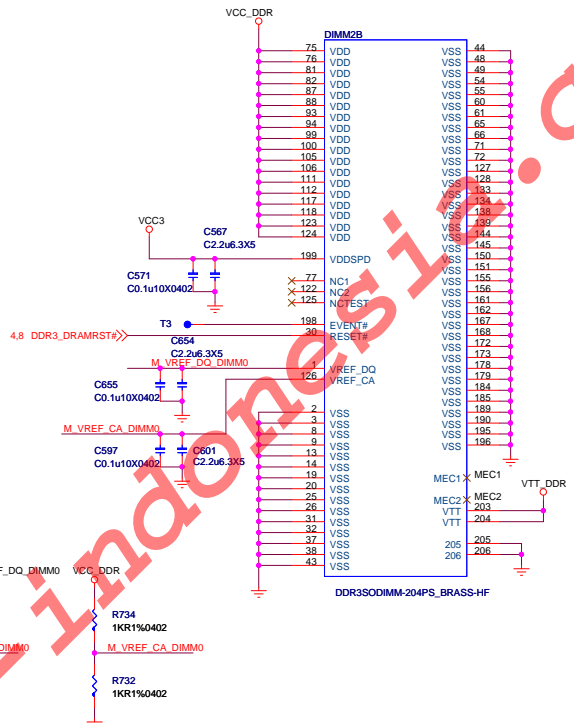
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SODIMM#A

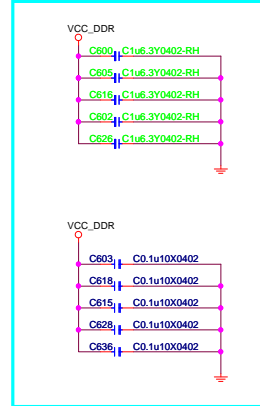
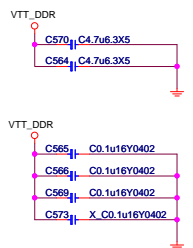



ADDRESS: 000
0xA0

H=5.2mm



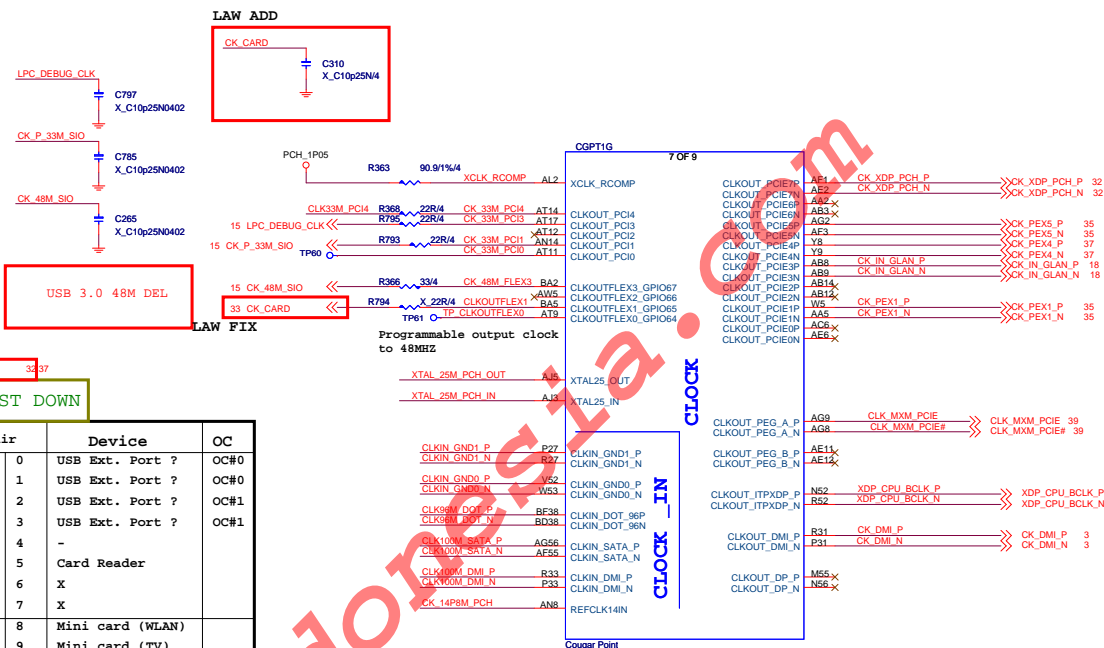
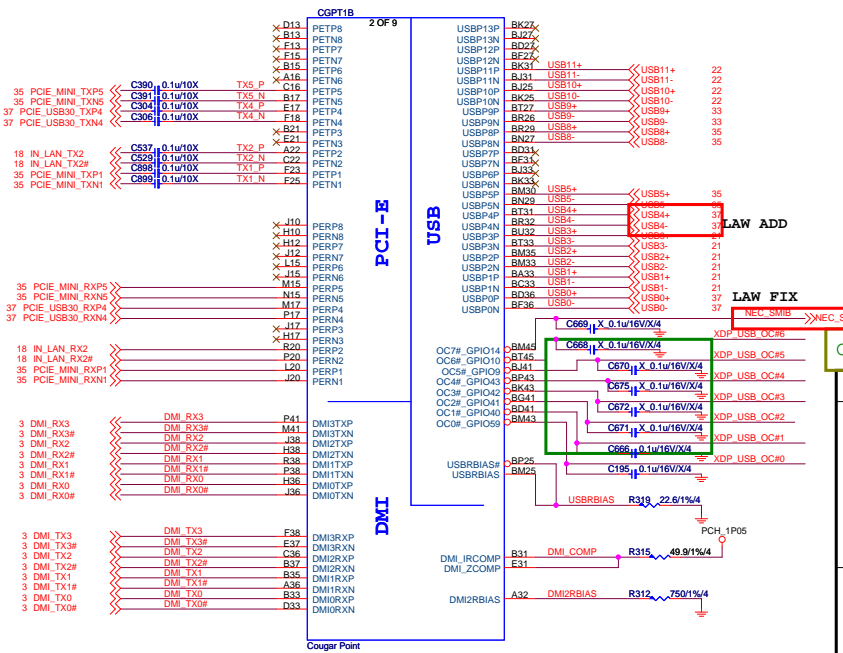
CHANNEL A V_SM_VTT DECOUPLING CAPS





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H61 SKU:PCIe ports 7 and 8 are disabled.
H61 SKU:USB ports 6, 7, 12 and 13 are disabled.



Pair	Device		OC
EHC1 #1	0	USB Ext. Port ?	OC#0
	1	USB Ext. Port ?	OC#0
	2	USB Ext. Port ?	OC#1
	3	USB Ext. Port ?	OC#1
	4	-	
	5	Card Reader	
	6	X	
	7	X	
EHC1 #2	8	Mini card (WLAN)	
	9	Mini card (TV)	
	10	Webcam	
	11	Touch Screen	
	12	X	
	13	X	

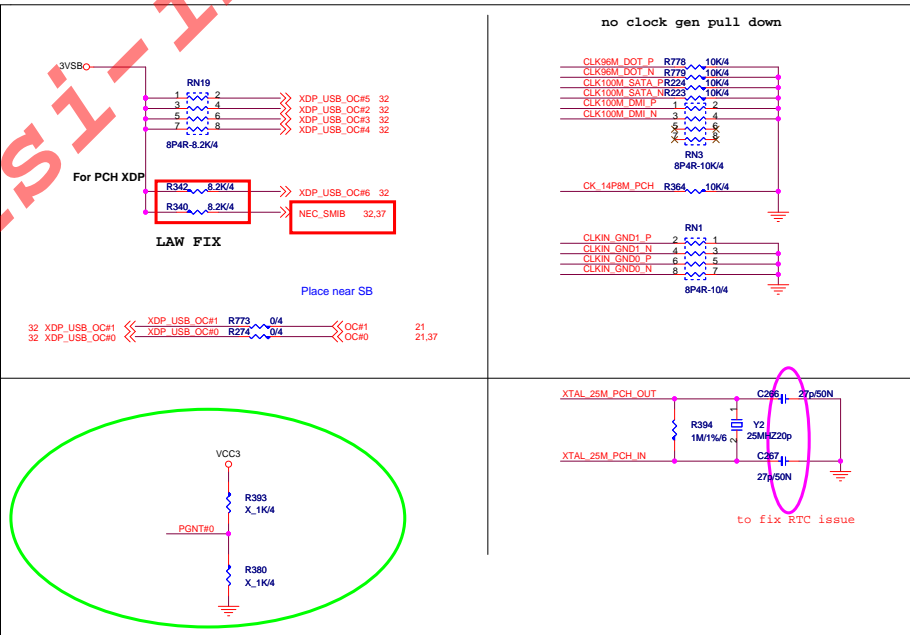
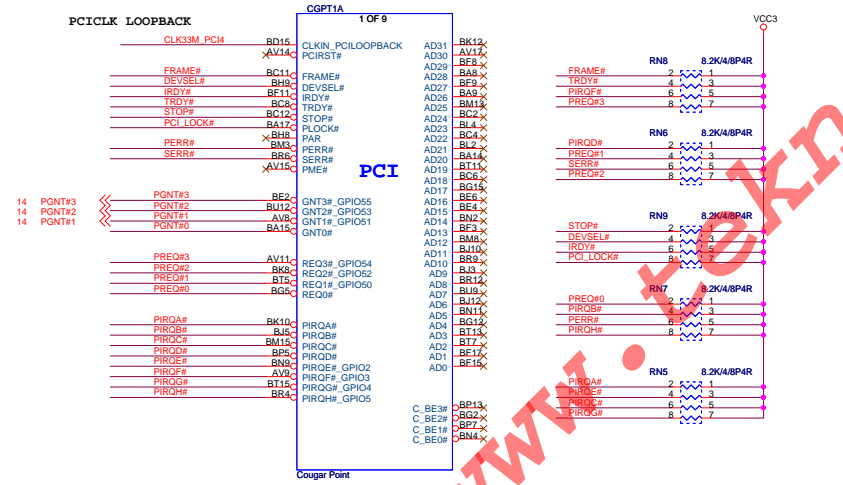
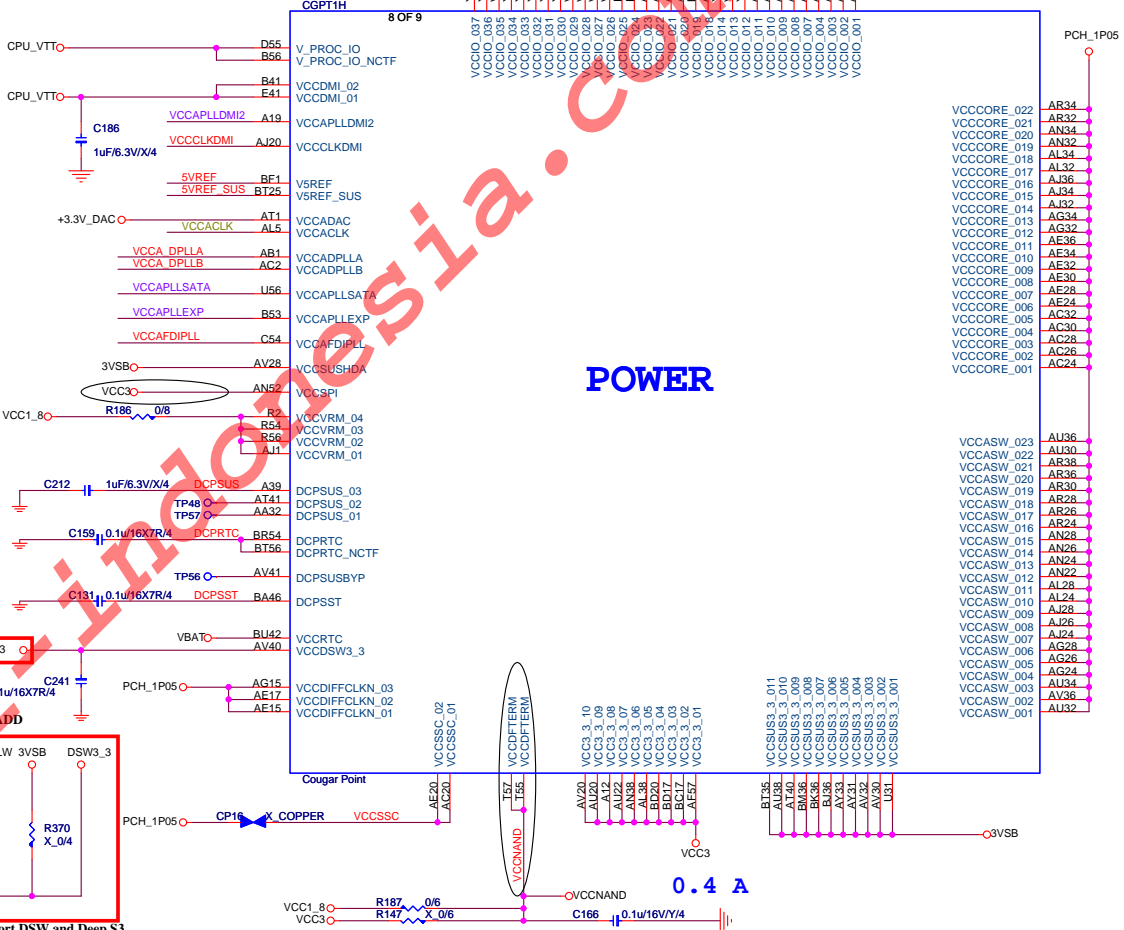
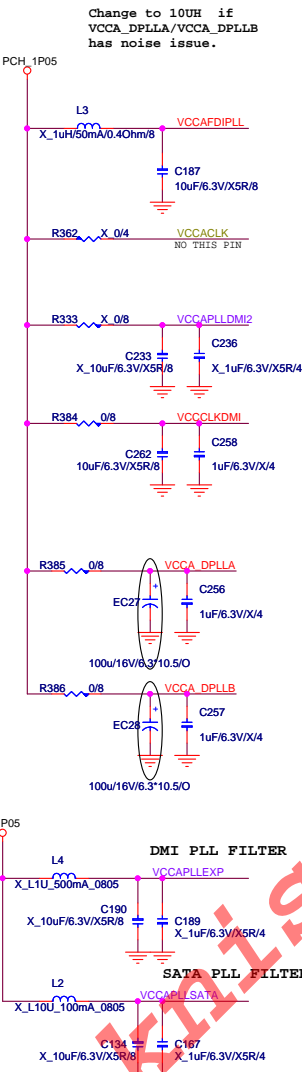
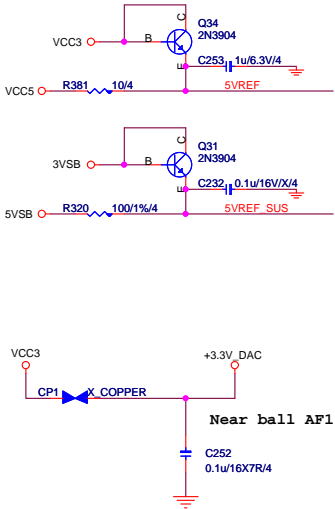




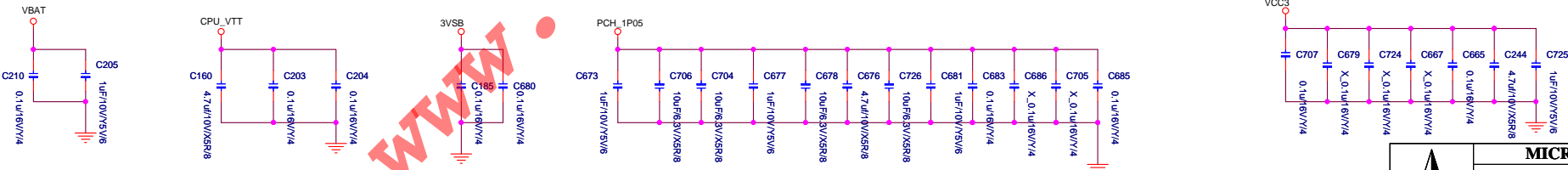
Table 3-7. VCCPLL Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Electrolytic 220µF	1	77mΩ	3.3nH	Output	North of processor - as close to RM keep-out as possible	1
10µF 0805 XSR	1	3mΩ	0.51nH	Output		1,2,3

5VREF & 5VREF_SUS Sequencing Circuit

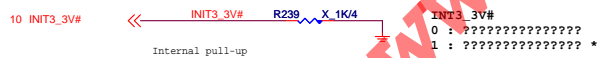
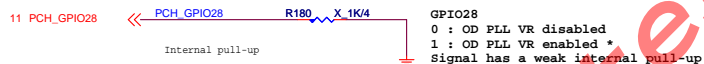
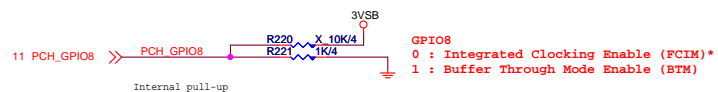
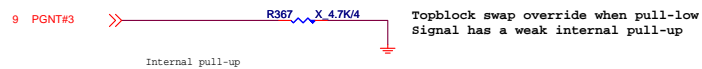
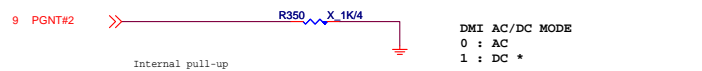
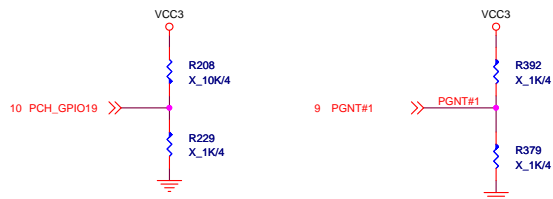


PCH decoupling cap

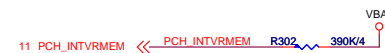


CP REQUIRED STRAPS

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating



1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.

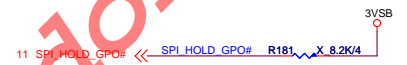


HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

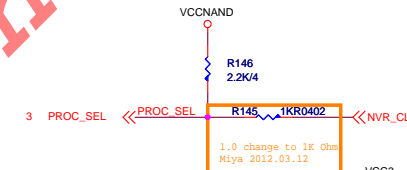


HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

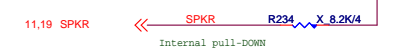
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



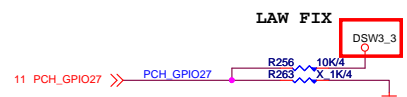
GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



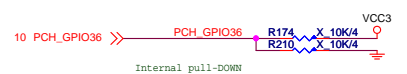
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



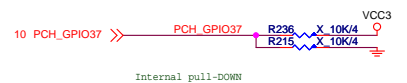
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.
If not used, require a weak pull-up(8.2k-10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high



Cougar point EDS PAGE:93 This signal should not be pull high

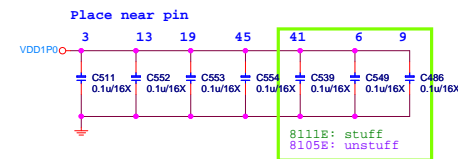
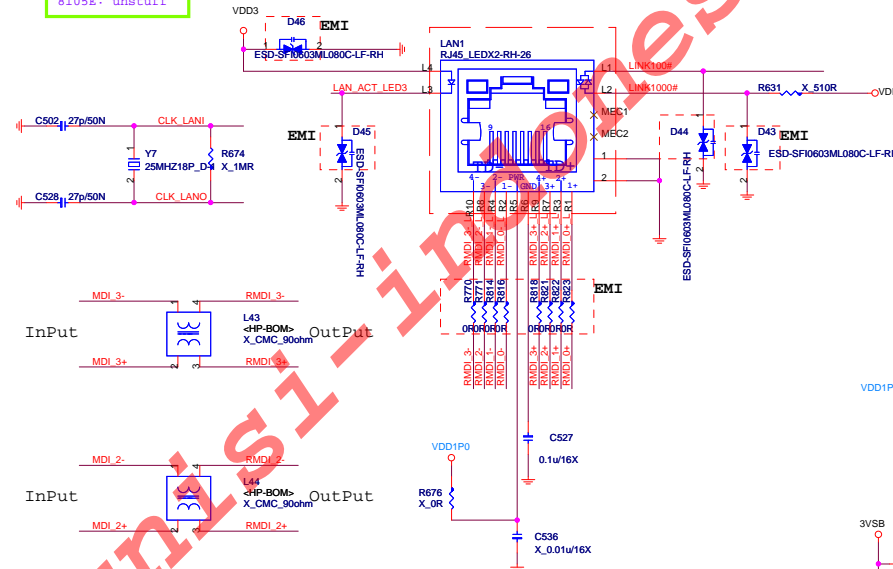
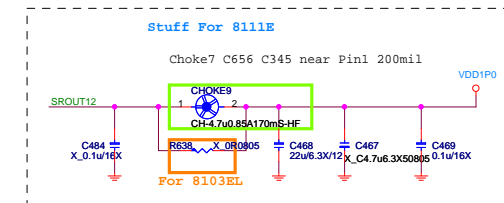
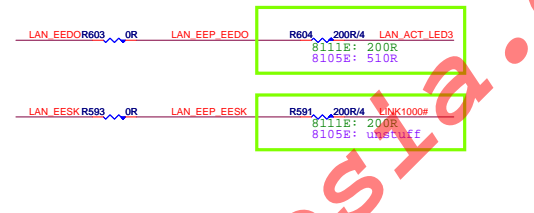
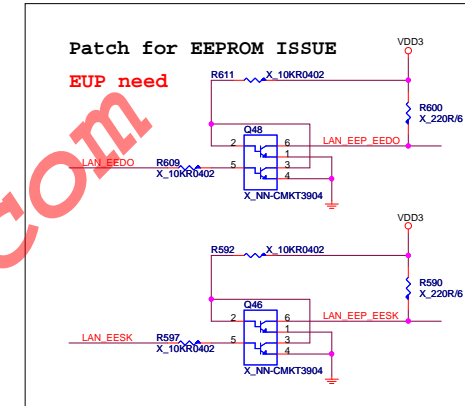
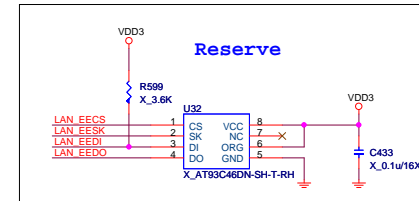
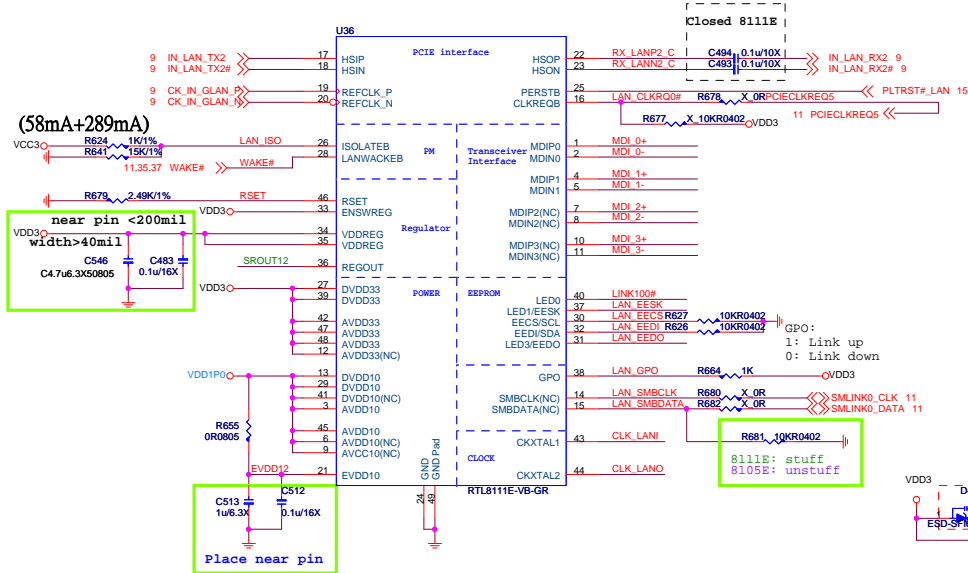


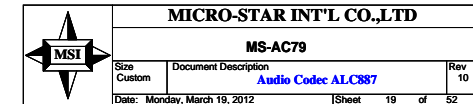
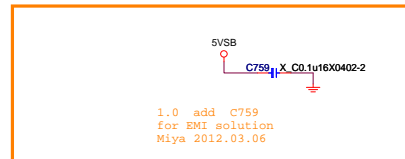
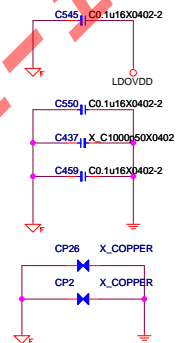
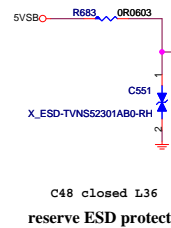
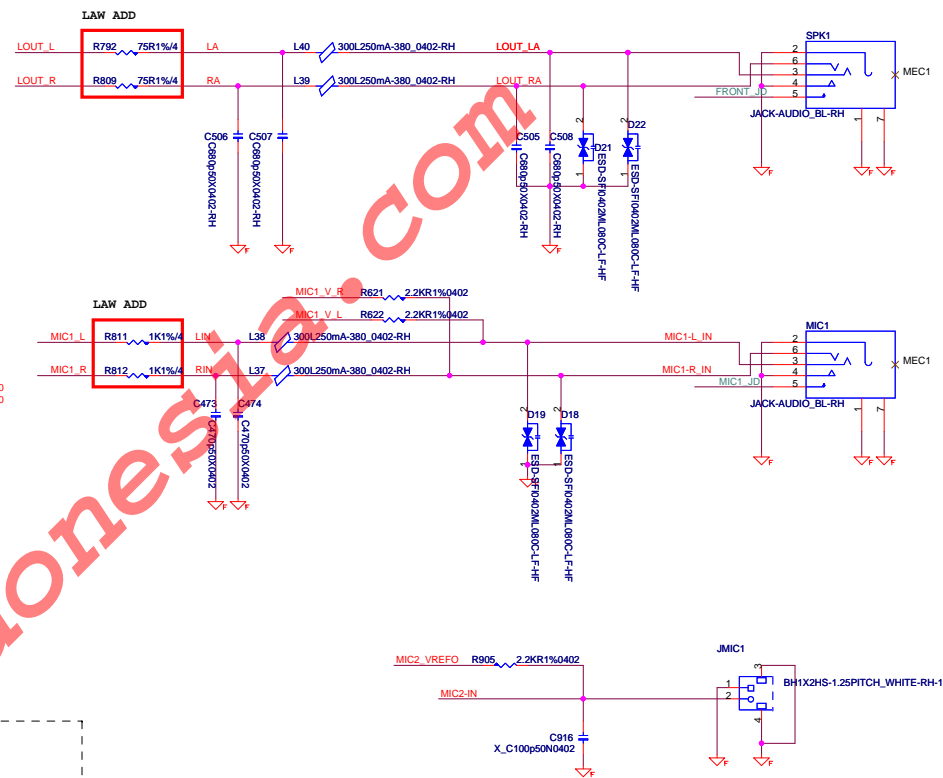
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PCH

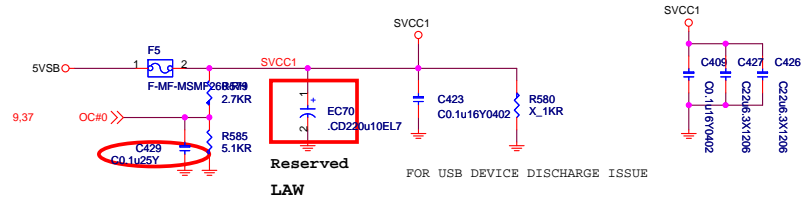
GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPI00	BMBUSY#	I/O	CORE	Y	3.3V	GPI	NEC_SMIB	Pull-up 10K to VCC3	GPI
GPI01		I/O	CORE	Y	3.3V	GPI	WLAN2_PWRON		GPO
GPI02	PIRQE#	I/OD	CORE	Y	5V	GPI	PIRQE#	Pull-up 8.2K to VCC3	No USE
GPI03	PIRQF#	I/OD	CORE	Y	5V	GPI	PIRQF#	Pull-up 8.2K to VCC3	No USE
GPI04	PIRQG#	I/OD	CORE	Y	5V	GPI	PIRQG#	Pull-up 8.2K to VCC3	No USE
GPI05	PIRQH#	I/OD	CORE	Y	5V	GPI	PIRQH#	Pull-up 8.2K to VCC3	No USE
GPI06		I/O	CORE	Y	3.3V	GPI	BKLT-	Pull-up 10K to VCC3	GPI
GPI07		I/O	CORE	Y	3.3V	GPI	BKLT+	Pull-up 10K to VCC3	GPI
GPI08	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	PCH_GPIO8	Pull-down 1K to GND	No USE
GPI09	OC5#	I/O	Suspend	Y	3.3V	Native	OC5#	Pull-up 10K to 3VSB	Native
GPI010	OC6#	I/O	Suspend	Y	3.3V	Native	OC6#	Pull-up 10K to 3VSB	Native
GPI011	SMBALERT#	I/O	Suspend	Y	3.3V	Native	PCH_GPIO11	Pull-up 10K to 3VSB	No USE
GPI012	LAN_PHY_PWR_CTRL	I/O	Suspend	Y	3.3V	Native	(NC)		No USE
GPI013	HDA_DOCK_RST#	I/O	Suspend	Y	3.3V	GPI	SIO_PME#		No USE
GPI014	OC7#	I/O	Suspend	Y	3.3V	Native	OC7#	Pull-up 10K to 3VSB	Native
GPI015	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	SPI_HOLD_GPO#	Internal pull-down	Straps
GPI016	SATA4GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO16	Pull-up 10K to VCC3	No USE
GPI017		I/O	CORE	N	3.3V	GPI	WLAN_PWRON	Pull-up 10K to VCC3	GPO
GPI019		I/O	CORE	N	3.3V	GPI	PCH_GPIO19	Internal pull-up	Straps
GPI020	PCIECLKRQ2#	I/O	CORE	N	3.3V	Native	PCH_GP20	Pull-down 10K to GND	Native
GPI021	SATA0GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO21	Pull-up 10K to VCC3	No USE
GPI022	SCLOCK	I/O	CORE	N	3.3V	GPI	PCH_GPIO22	Pull-up 10K to VCC3	No USE
GPI023	LDRQ1#	I/O	CORE	N	3.3V	Native	(NC)		No USE
GPI024	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PCH_GPIO24	Pull-up 10K to 3VSB	No USE
GPI025	PCIECLKRQ3#	I/O	Suspend	N	3.3V	Native	USB3_CLKRQ#	Pull-up 10K to 3VSB	Native
GPI026	PCIECLKRQ4#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ4#	(pull high)	Native
GPI027	Unmultiplexed	I/O	Deep Sleep	N	3.3V	GPI	DSW_WAKE#	internal pull-up	GPI
GPI028	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PLL_ODVR_EN	internal pull-up	Straps
GPI029	SLP_LAN#	I/O	Suspend	N	3.3V	GPI	SLP_LAN#	Pull-up 10K to 3VSB	No USE
GPI030	SUSPWRDNACK	I/O	Deep Sleep	N	3.3V	Native	SUSPWRACK	Pull-up 10K to 3VSB	Native
GPI031	ACPRESENT	I/O	Deep Sleep	N	3.3V	GPI	AC_PRESENT	Pull-up 10K to 3VSB	No USE
GPI032	CLKRUN#	I/O	CORE	N	3.3V	GPO	PM_CLKRUN#	Pull-up 8.2K to VCC3	
GPI033	HDA_DOCK_EN#	I/O	CORE	N	3.3V	GPO	HDA_DOCK_EN#	Test Pin	No USE
GPI034	STP_PCI#	I/O	CORE	N	3.3V	GPI	STP_PCI#	Pull-up 10K to VCC3	No USE
GPI035	(Mobile Only)	I/O	CORE	N	3.3V	GPO	PCH_GPIO35	Test Pin	No USE
GPI036	SATA2GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO36	Pull-down 10K to GND	Straps
GPI037	SATA3GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO37	Pull-down 10K to GND	Straps
GPI038	SLOAD	I/O	CORE	N	3.3V	GPI	PCH_GPIO38	Pull-up 10K to VCC3	No USE
GPI039	SDATAOUT0	I/O	CORE	N	3.3V	GPI	GFX_DET		GPI
GPI040	OC1#	I/O	Suspend	N	3.3V	Native	USB_OC1#	(pull high)	Native



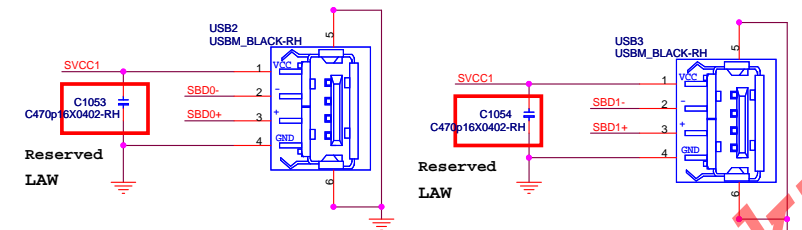
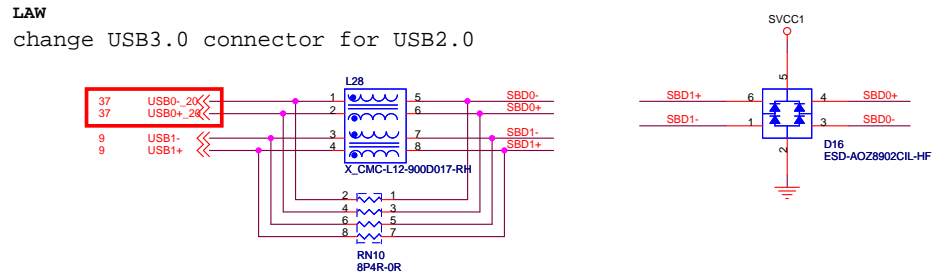




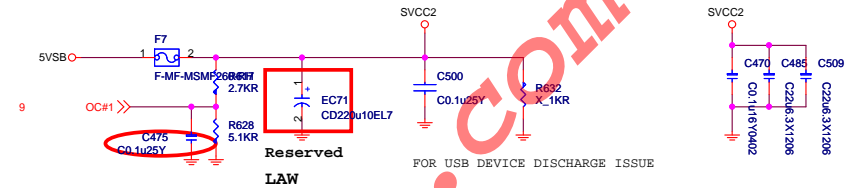
POWER CIRCUIT FOR USB PORT 0,1 (REAR)



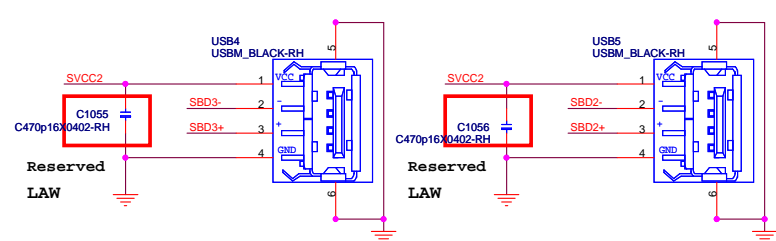
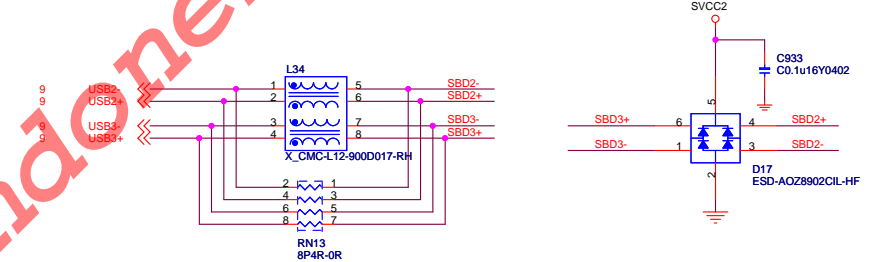
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



POWER CIRCUIT FOR USB PORT 2,3 (REAR)

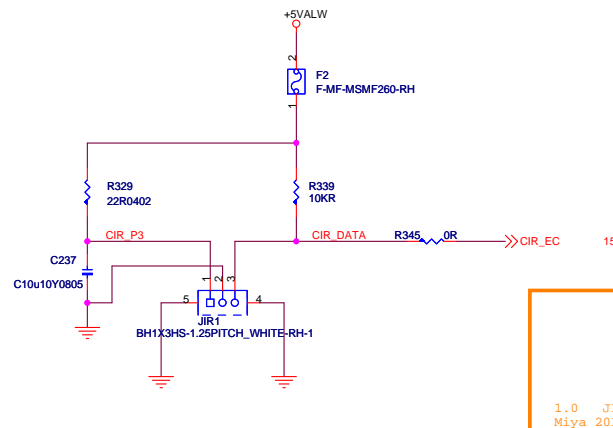


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

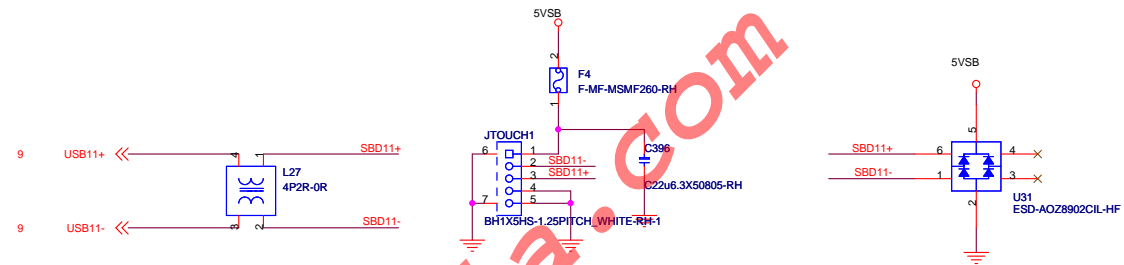


MICRO-STAR INT'L CO.,LTD			
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Custom	USB CONNECTOR	10	
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IR

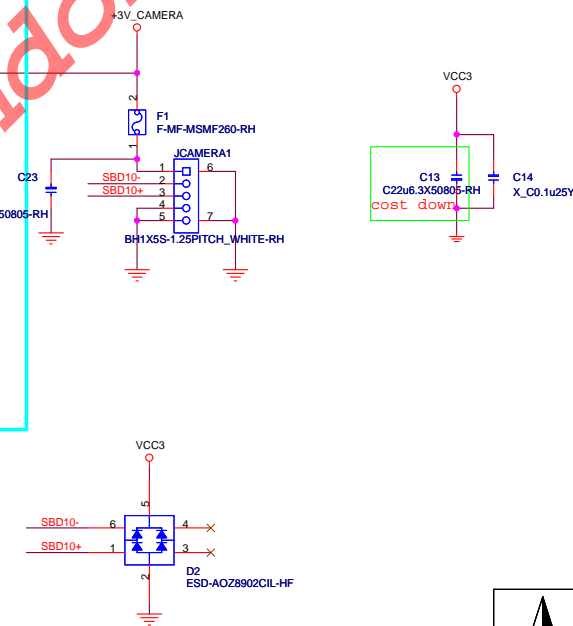
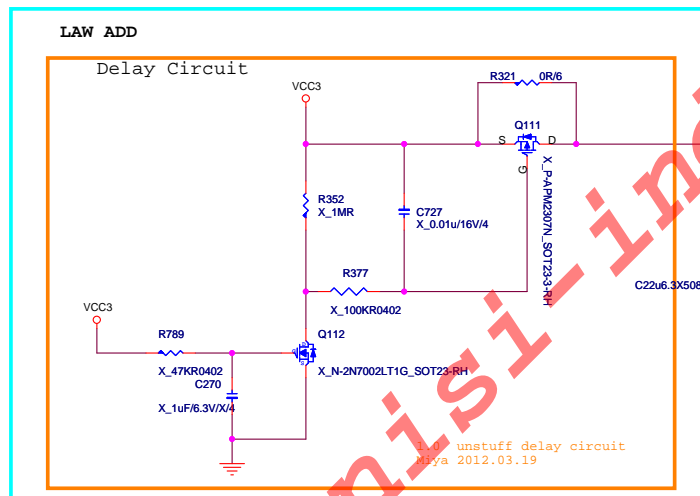


Multi Touch



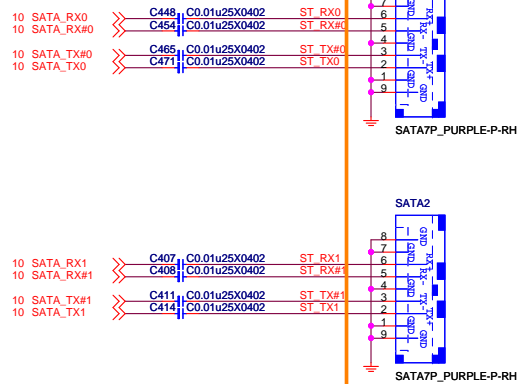
Webcam

BOM先預留!!
之後再拿掉



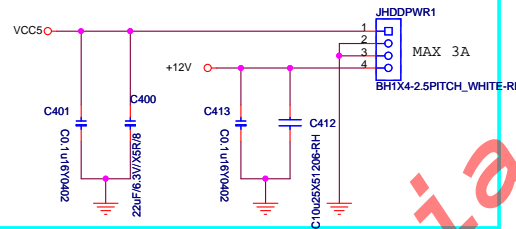
MICRO-STAR INT'L CO.,LTD			
MS-AC79			
Size	Document Description	Rev	
Custom	Multi Touch / Webcam / IR	10	
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SATA HDD

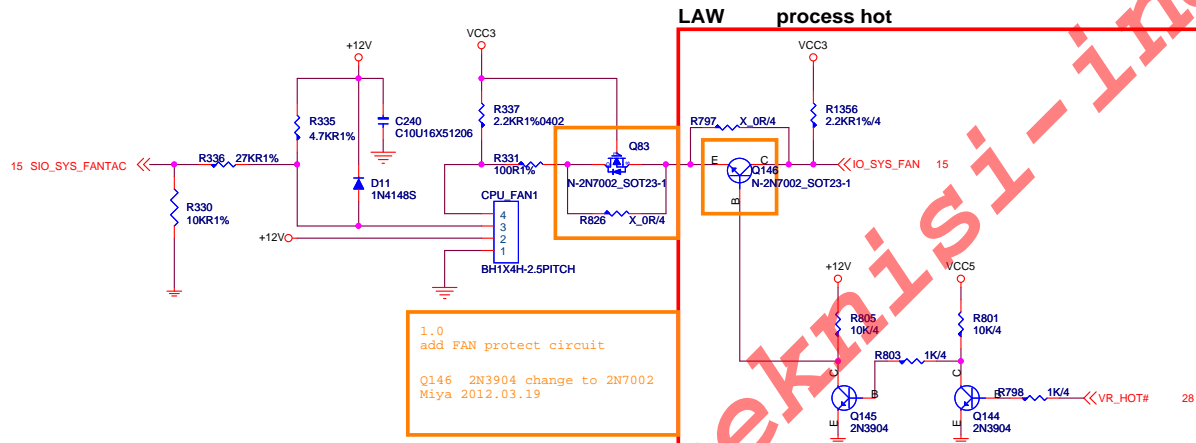


1.0 modify SATA connector Location name
2012.03.08

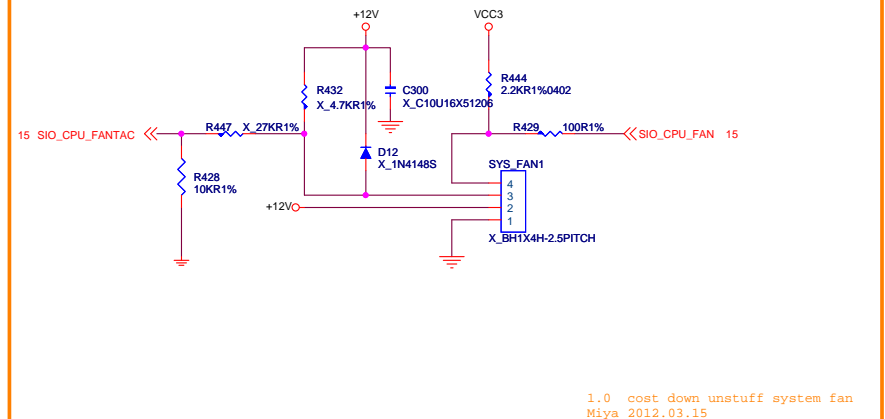
HDD & ODD Power



CPU FAN



SYSTEM FAN

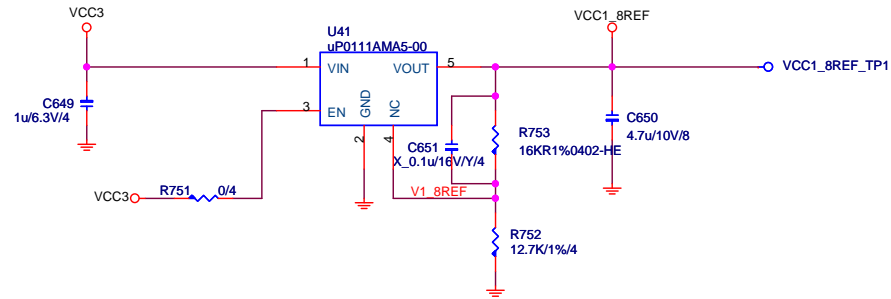


MICRO-STAR INT'L CO.,LTD

MS-AC79

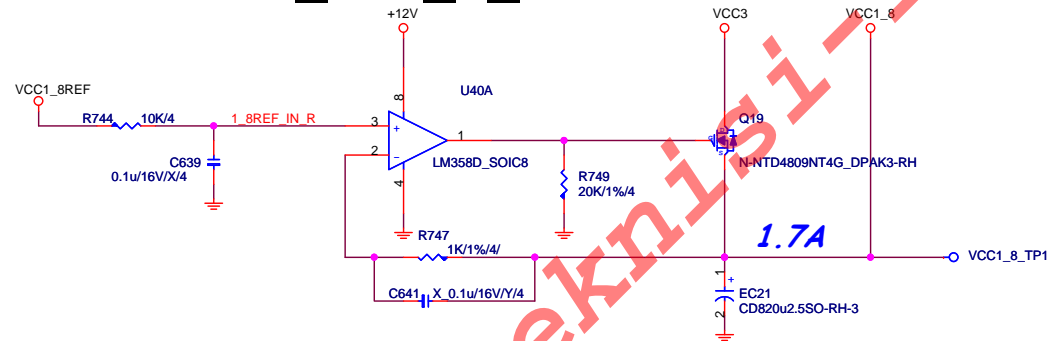
Size	Document Description	Rev
Custom	SATA /FAN Control	10
Date: Monday, March 19, 2012	Sheet 23 of 52	

VCC1_8REF



I31-0770709-U33 change I31-0111A09-U33 by law

CPU_PLL_1_8



MICRO-STAR INT'L CO.,LTD		
MS-AC79		
Size B	Document Description ACPI Controller UPI	Rev 10
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CPU_SA Power

VTT-->CPU_SA

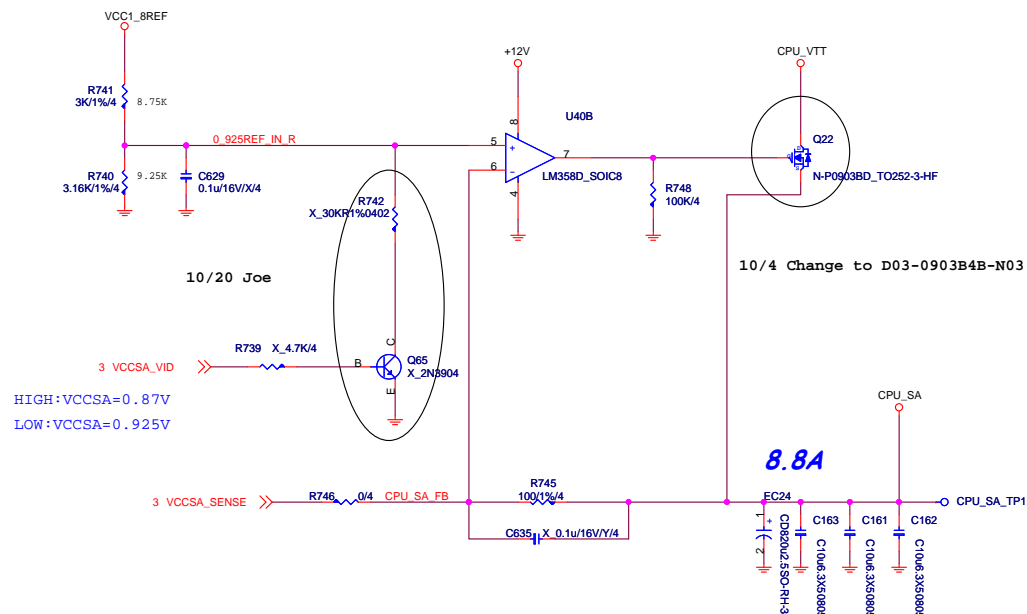


Table 3-10. VCCSA Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 500µF	1	7mΩ	1.4nH	Output	As close to RM keep-out as possible	1
10µF 0805 XSR	2	3mΩ	0.51nH	Output	Inside processor socket cavity	1,3

Waiting CPU_VTT Ready



CP Power

DDR-->PCH

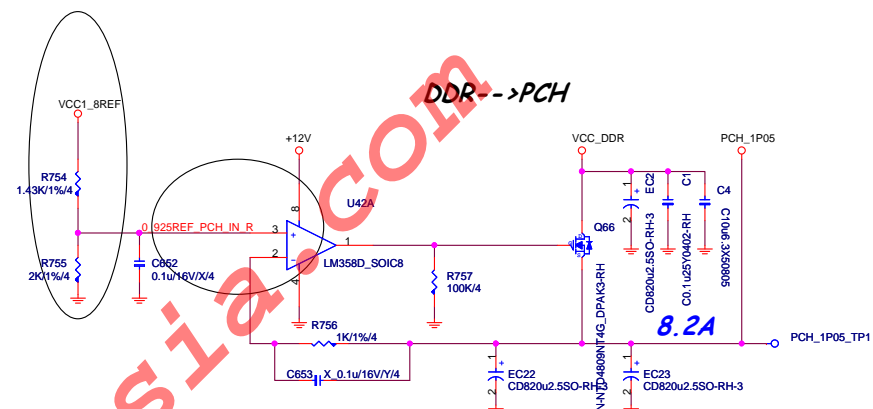
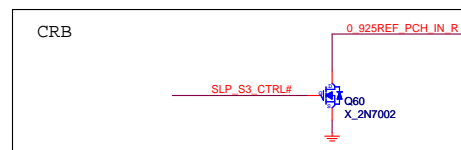


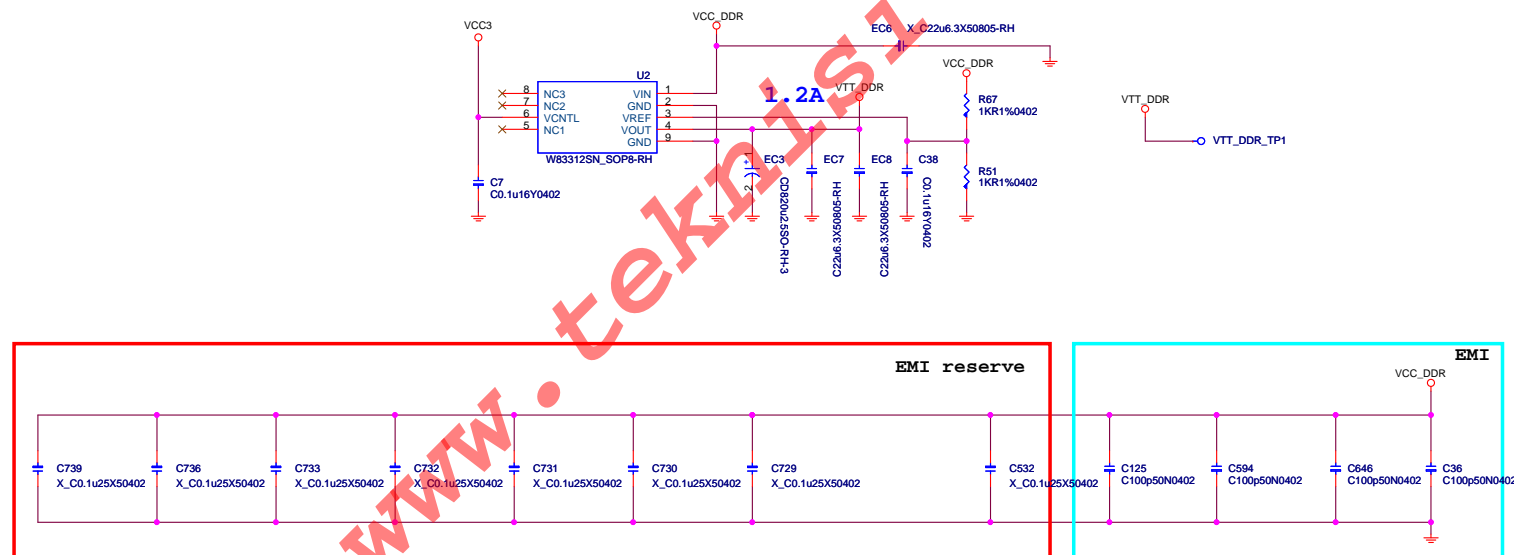
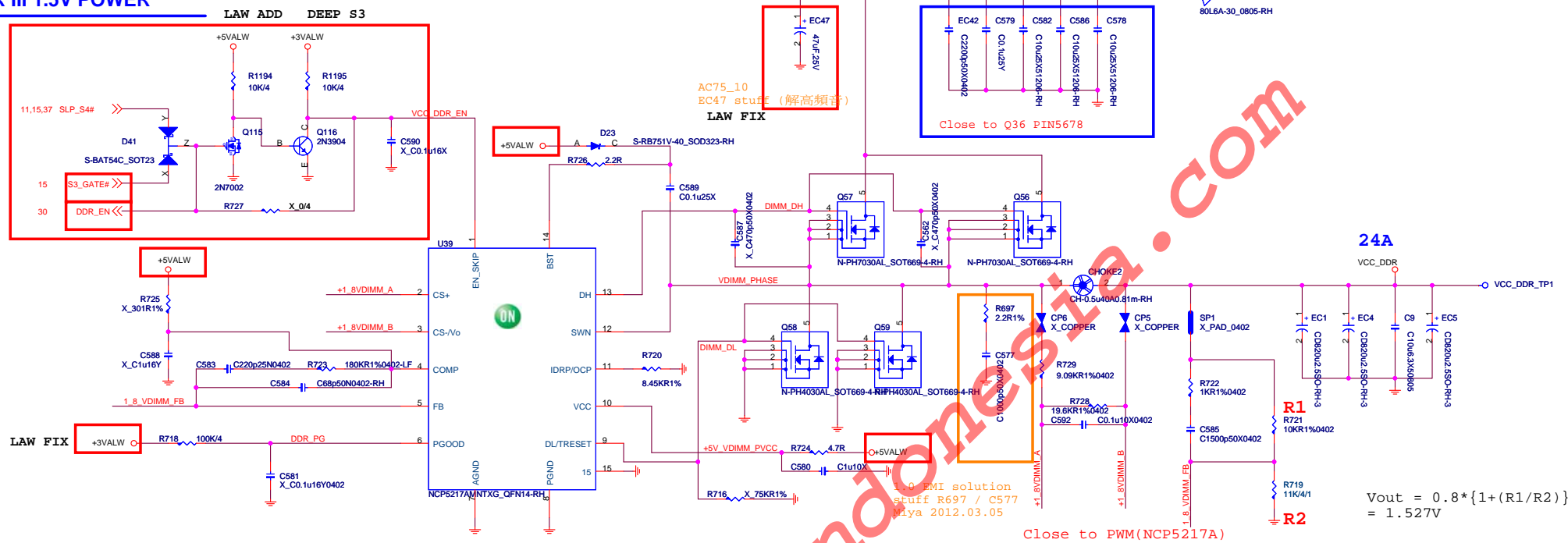
Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

Bulk Decoupling Location	Qty x µF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated)(AMT sku)	1x820µF	21mohm (bulk)
1.05A rail for VccASW (dedicated)(AMT sku)	2x22µF MLCC	
1.05S rail merge with 1.05A rail (non-AMT sku)	1x500µF 2x 22µF MLCC	7mohm (bulk)

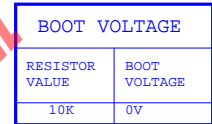
Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different than those shown.



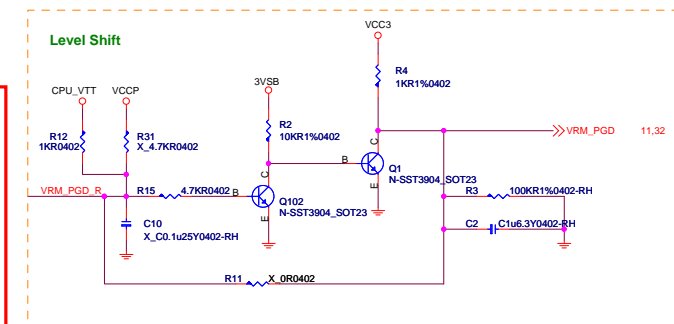
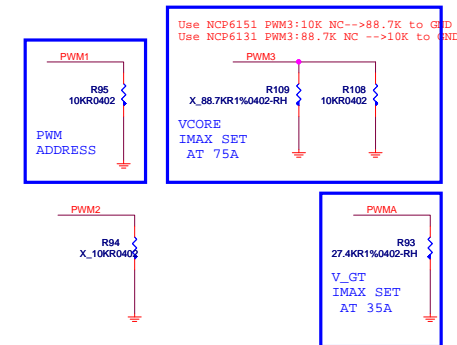
DDR III 1.5V POWER



PW	
RESISTOR VALUE	S



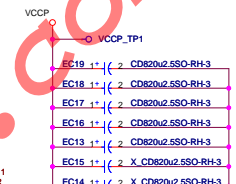
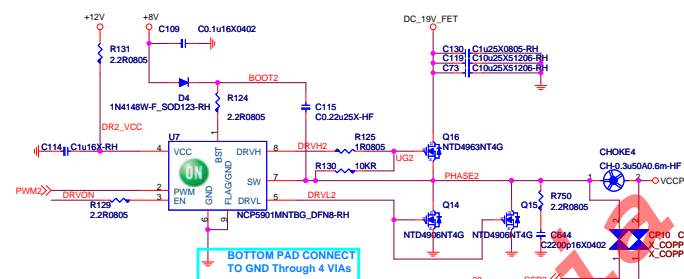
PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101



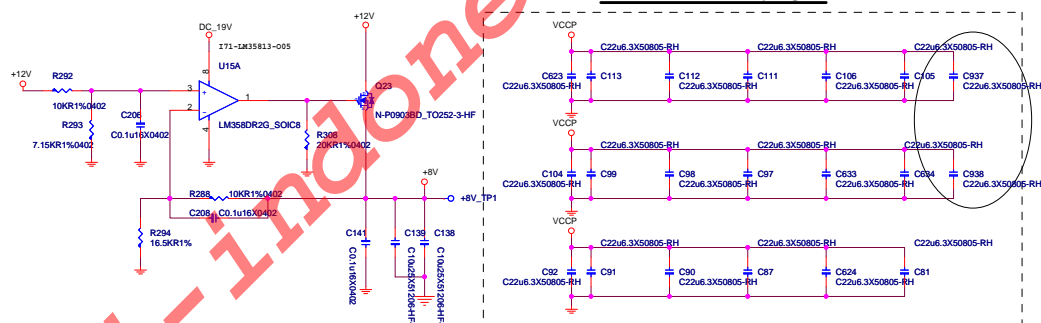
```
1.0 MOS change new MSI PN:
modify
Q13/Q16/Q20
Q11/Q12/Q14/Q15/Q17/Q18
Miya 2012.03.14
```

VCCP:75A

+CPU_VCCP Output Caps

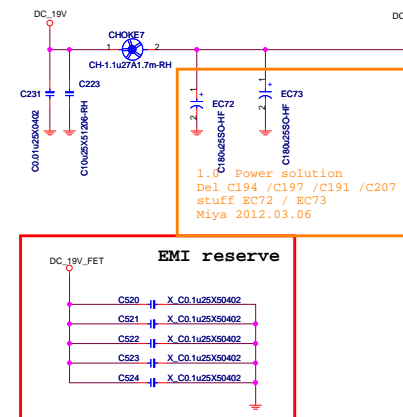
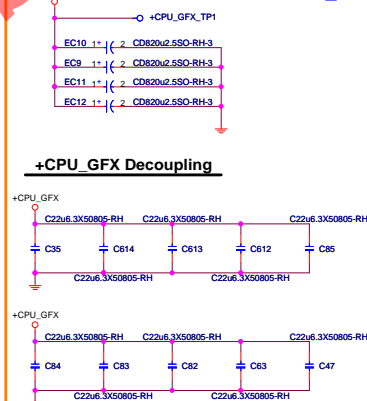


+CPU_VCCP-Decoupling



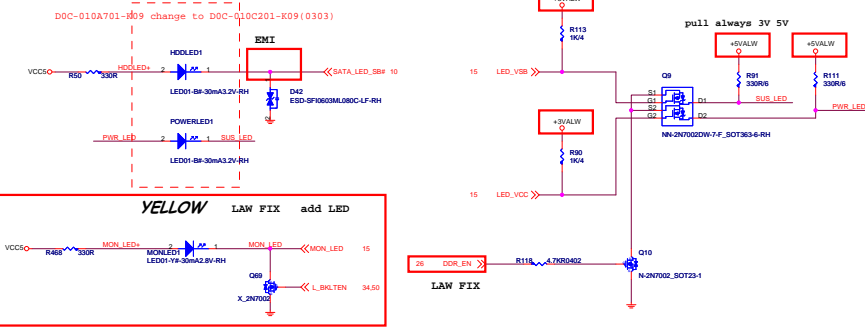
+CPU_GFX Output Caps

+CPU_GFX:35A



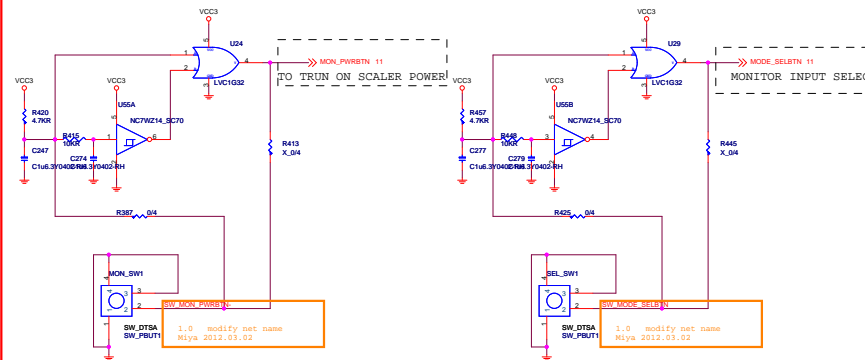
1.0 GPU SKU unstuff
Miya 2012.03.01

LED (for Fintek 71882)

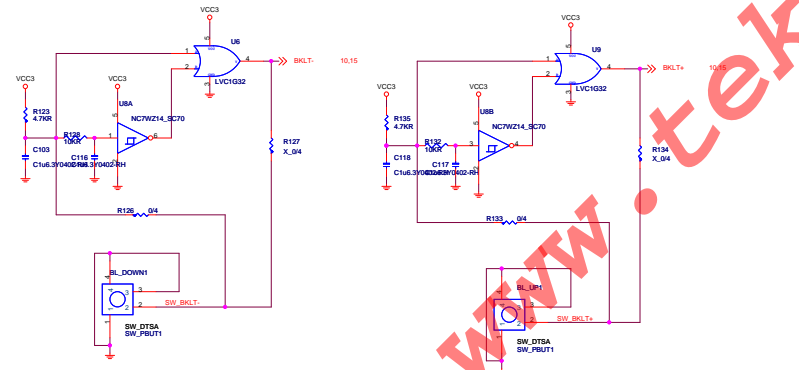


LAW DEL JSYSRST1

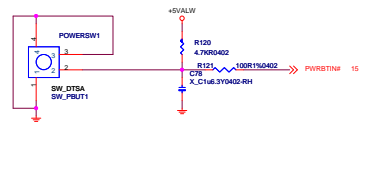
MONITOR ON/OFF BUTTON LAW FIX add button



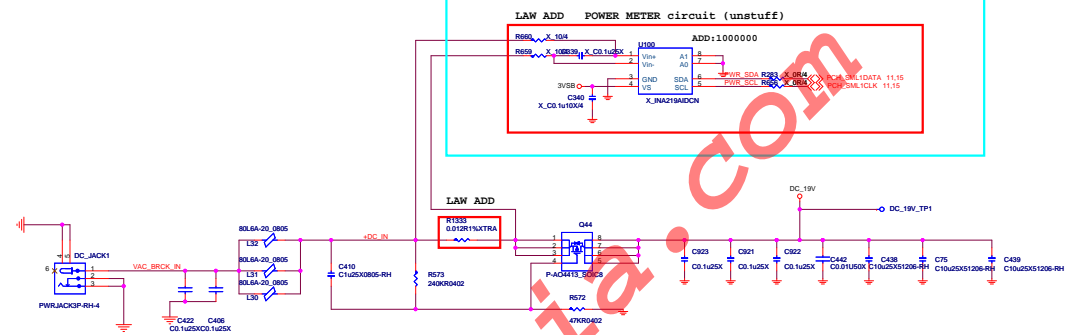
MODE SELECT CONTROL



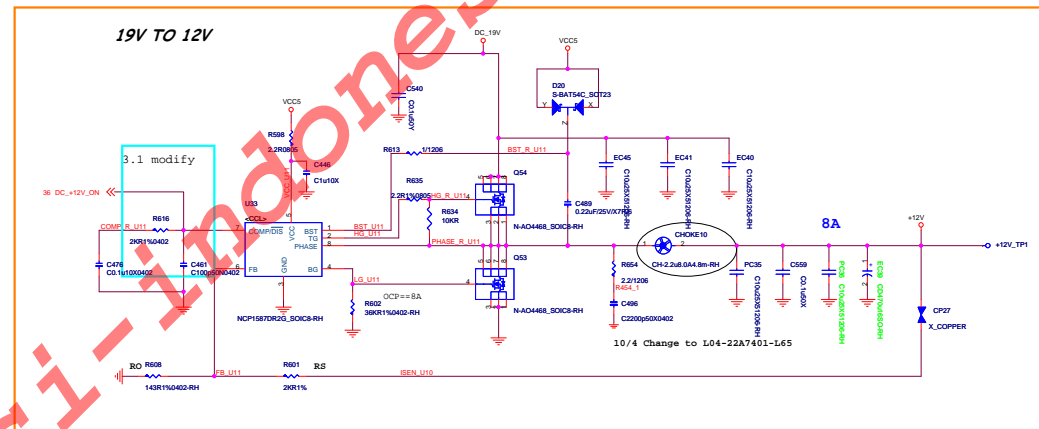
POWER ON/OFF BUTTON



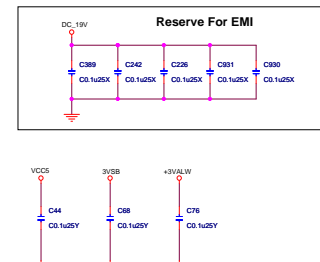
IGD試上件測FUNCTION



19V TO 12V



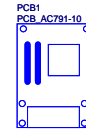
Reserve



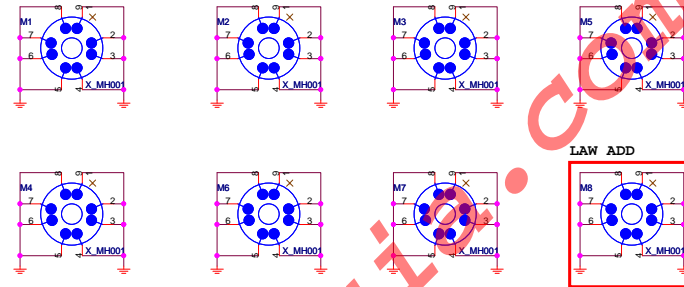
SB_SINK
footprint:HS_37_8X37_8

CPU1_X1
CPU SOCKET

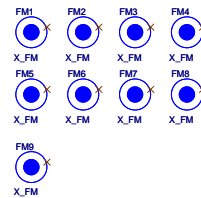
LAW ADD



Mounting Holes



Optical Fiducial Marks-120



BIOS label

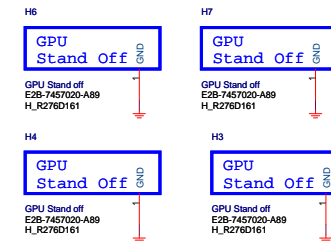


1.1 0706

VRM SINK



GPU Stand off

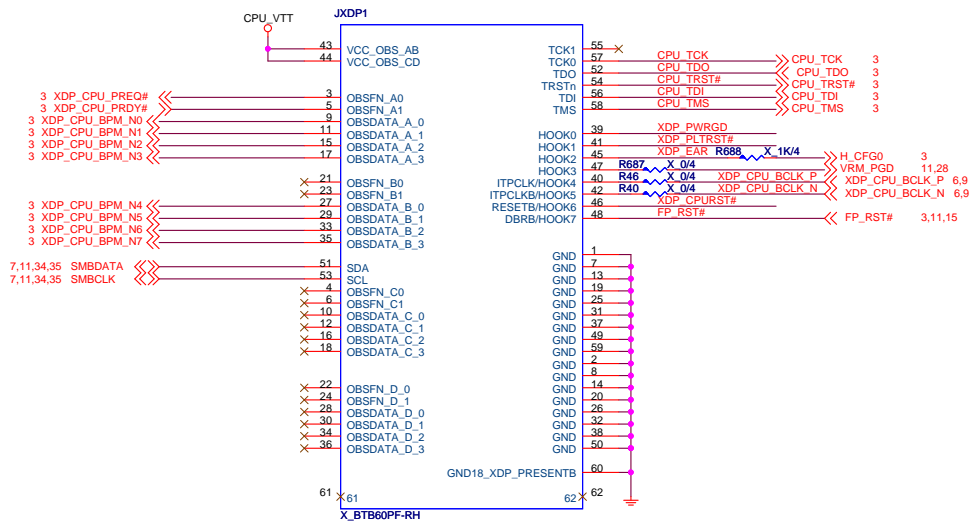


MICRO-STAR INT'L CO.,LTD

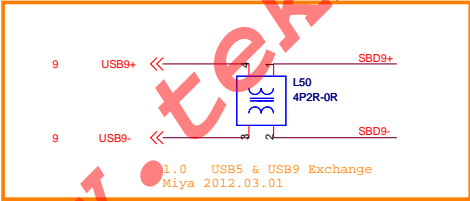
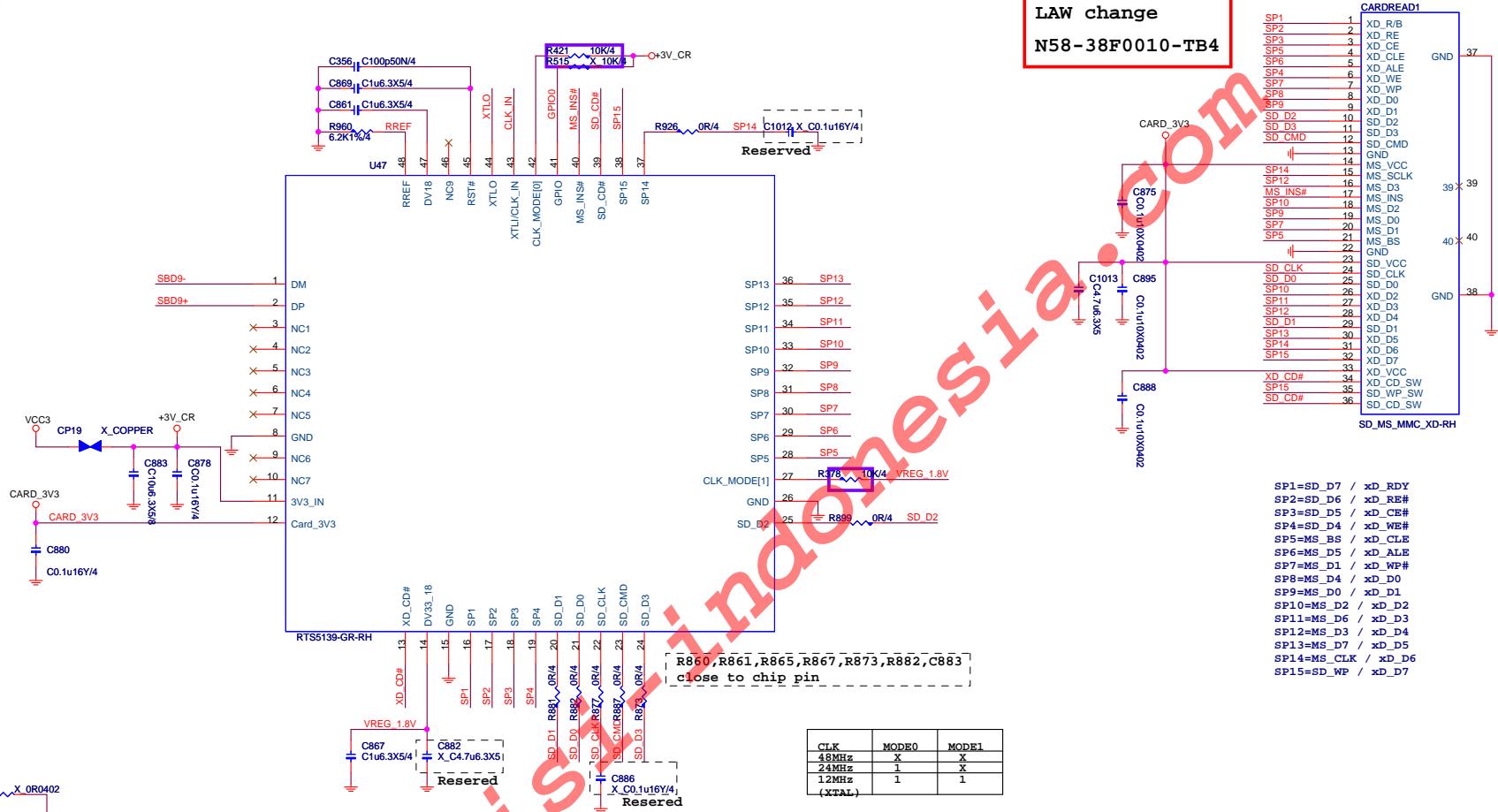
MS-AC79

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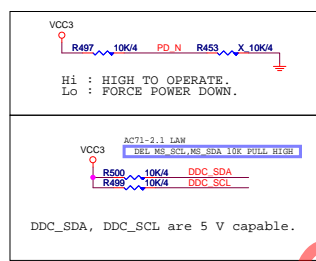
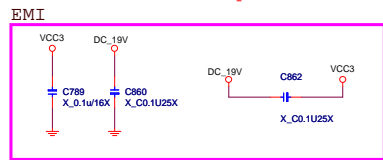
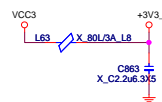
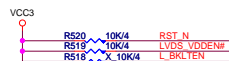
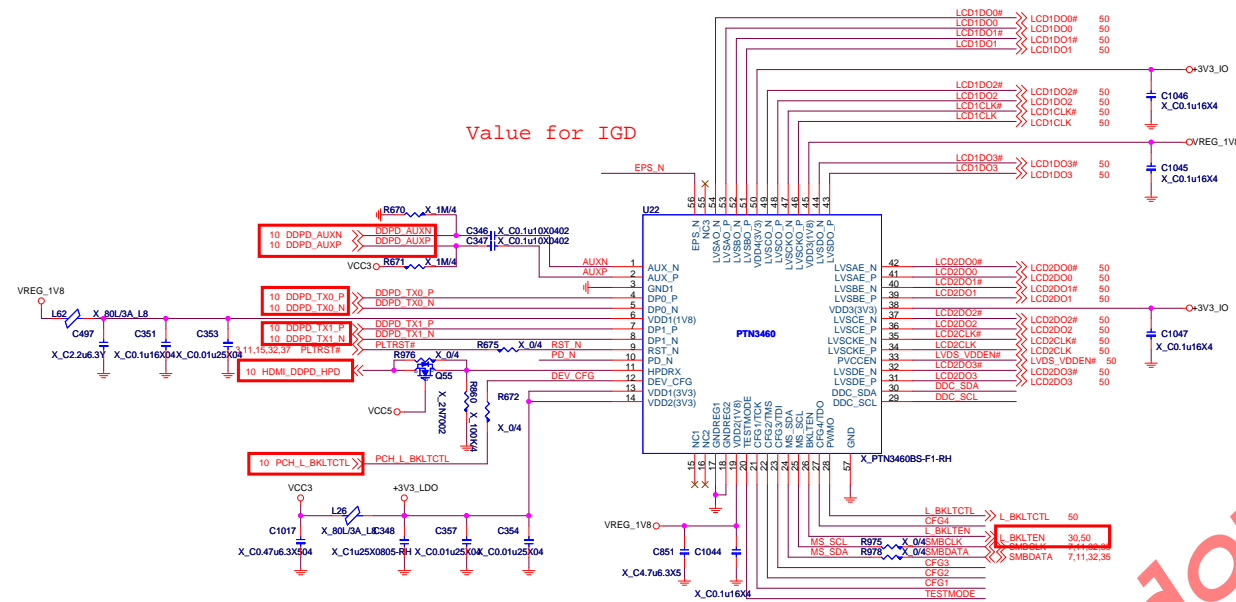
Reserve debug port 5020



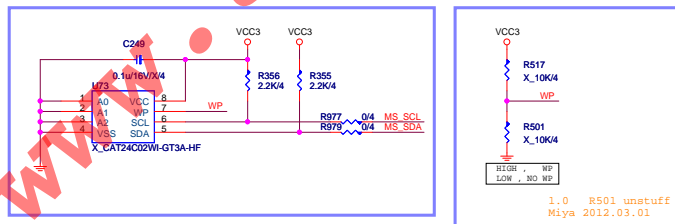
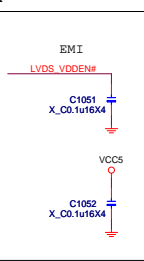
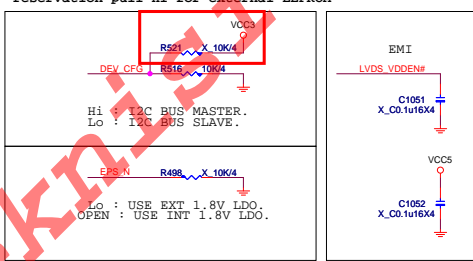
LAW change
N58-38F0010-TB4



Value for IGD



reservation pull HI for external EEPROM



VCC3

R458 X 10K/4 TESTMODE R463 X 10K/4

Hi : CFG[4:1]=JTAG PINS.
Lo : CFG[4:1]=CONFIG PINS.

CFG[4:1] function can fixed or set to GPIO by Firmware.

VCC3

R443 X 10K/4 CFG1 R451 X 10K/4

Vender default setting
Hi : DUAL LVDS BUS.
Lo : SINGLE LVDS BUS.

VCC3

R484 X 10K/4 CFG2 R475 X 10K/4

Vender default setting
Hi : JEIDA OR VESA FORMAT (18bpp).
OPEN : JEIDA FORMAT (24bpp).
Lo : VESA FORMAT (24bpp).

VCC3

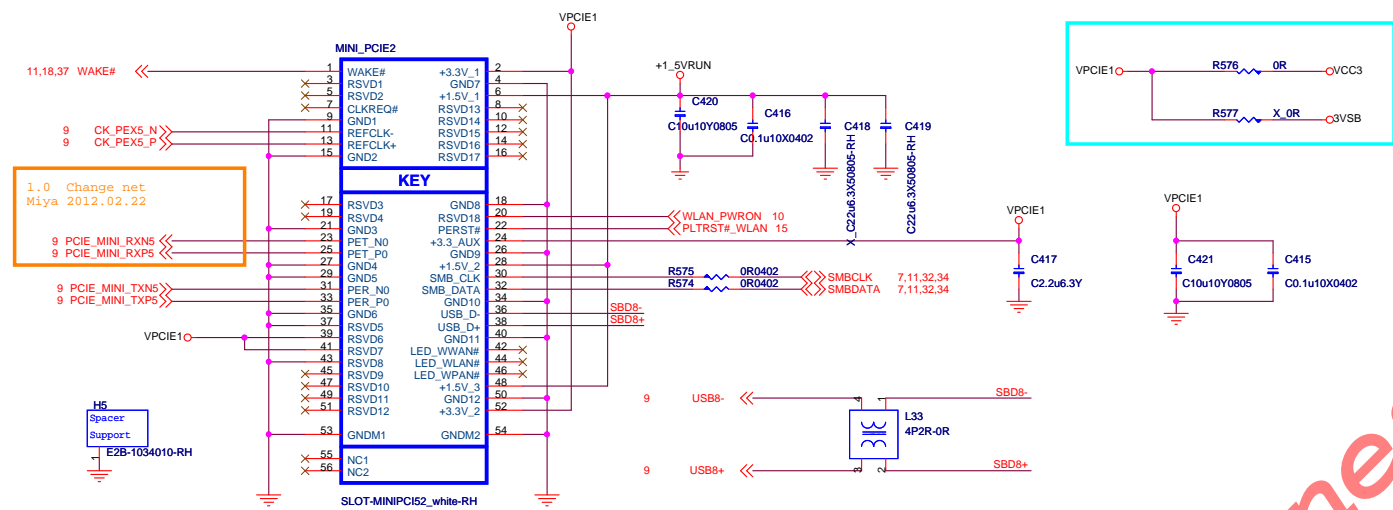
R496 X 10K/4 CFG3 R493 X 10K/4

Vender default setting
Hi : LVDS CLK FRQ 0.5%.
OPEN : LVDS CLK FRQ 1%.
Lo : LVDS CLK FRQ 0%.

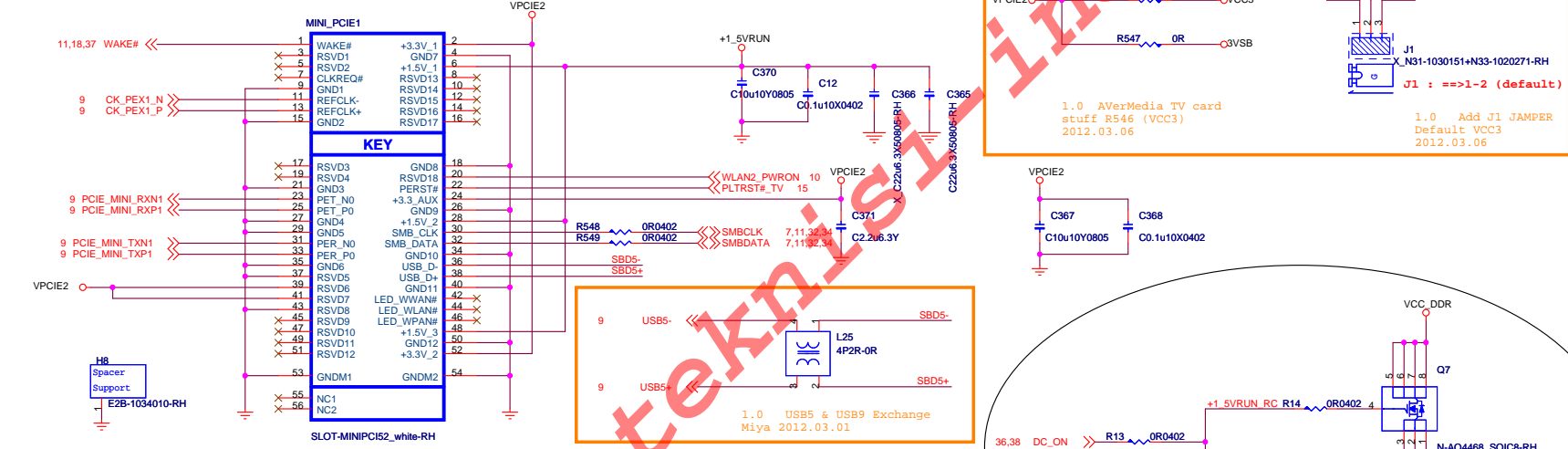
MSI define
PANEL ID0

	PANEL ID0	PANEL ID1
S1J-FELA006-S02 (LTM200KT10)	0	0
RESERVED	1	0
RESERVED	0	1
RESERVED	1	1

Wireless LAN(Short Card)

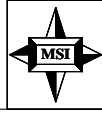


TV TUNER(Long Card)

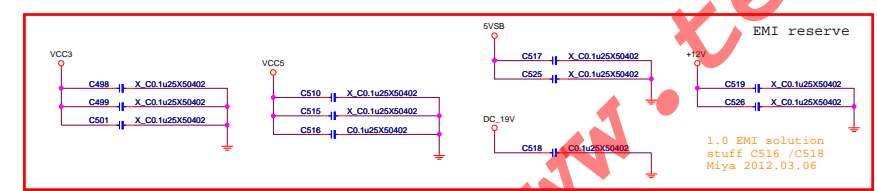
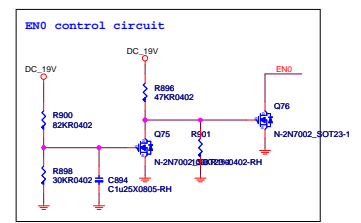
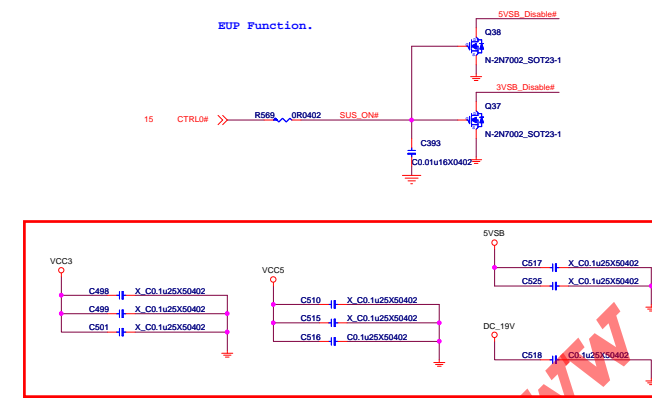
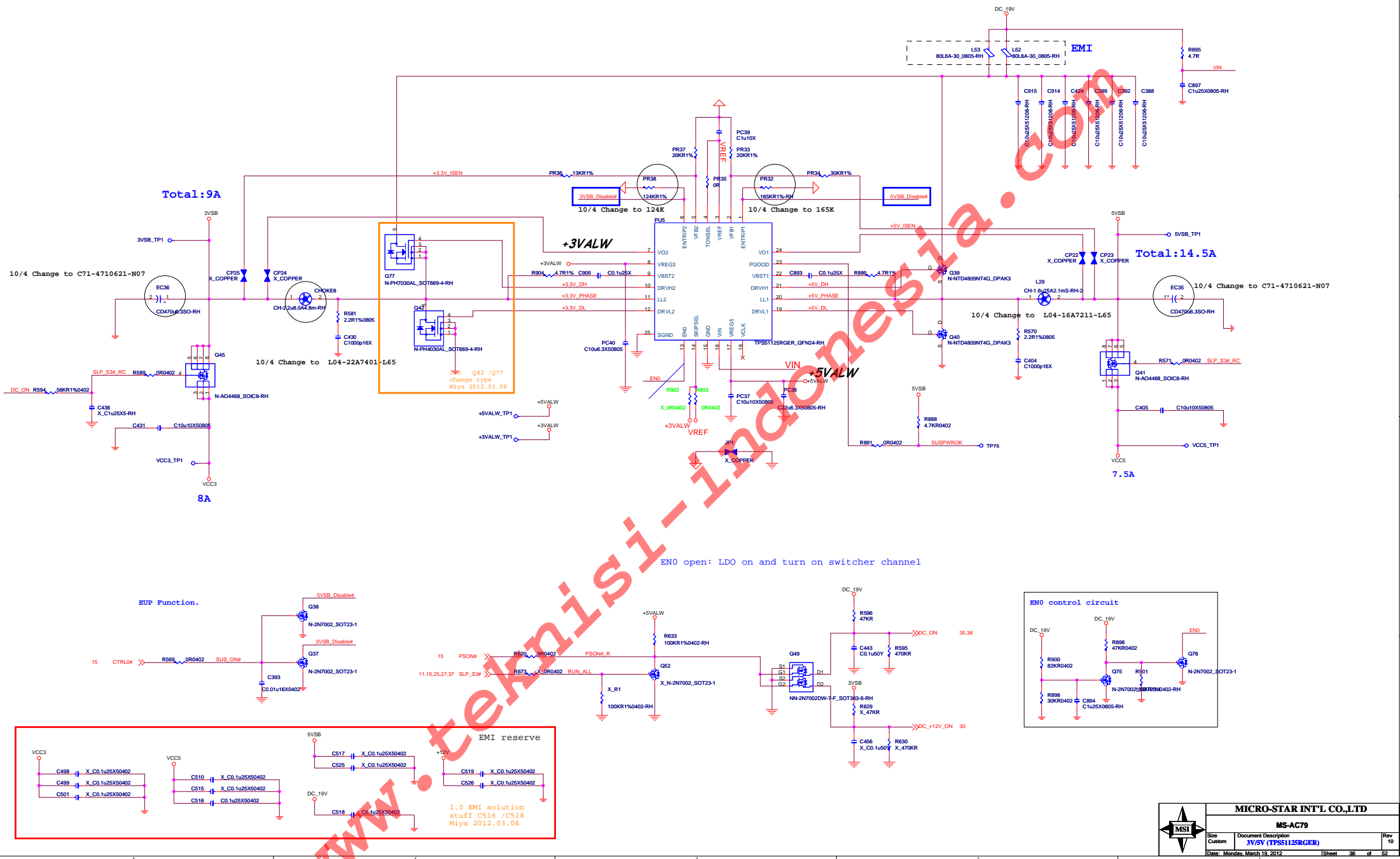


N11-0520040-A81

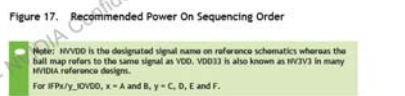
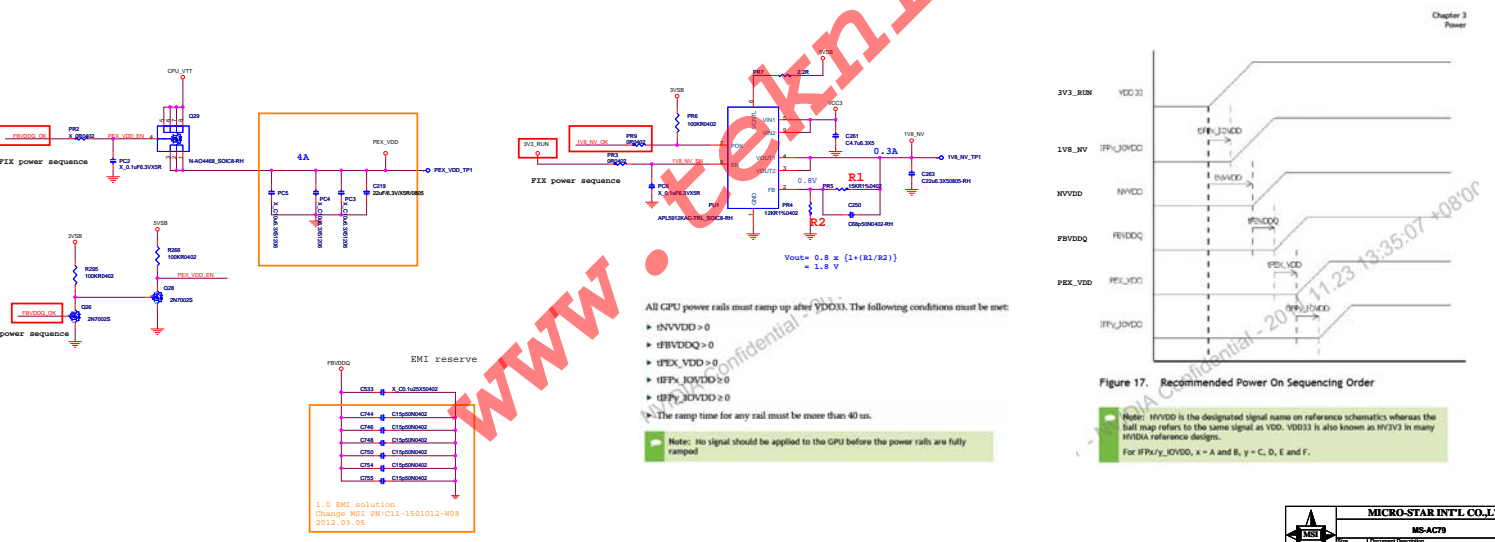
PCI ExpressR
Mini Card Electromechanical
Specification
Revision 1.2



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MS-AC79			
Size	Document Description	Rev	
Custom	3V/5V (TPS51125RGER)	10	
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According to N12x DG, please use 0.1uF on PCI-E AC cap.

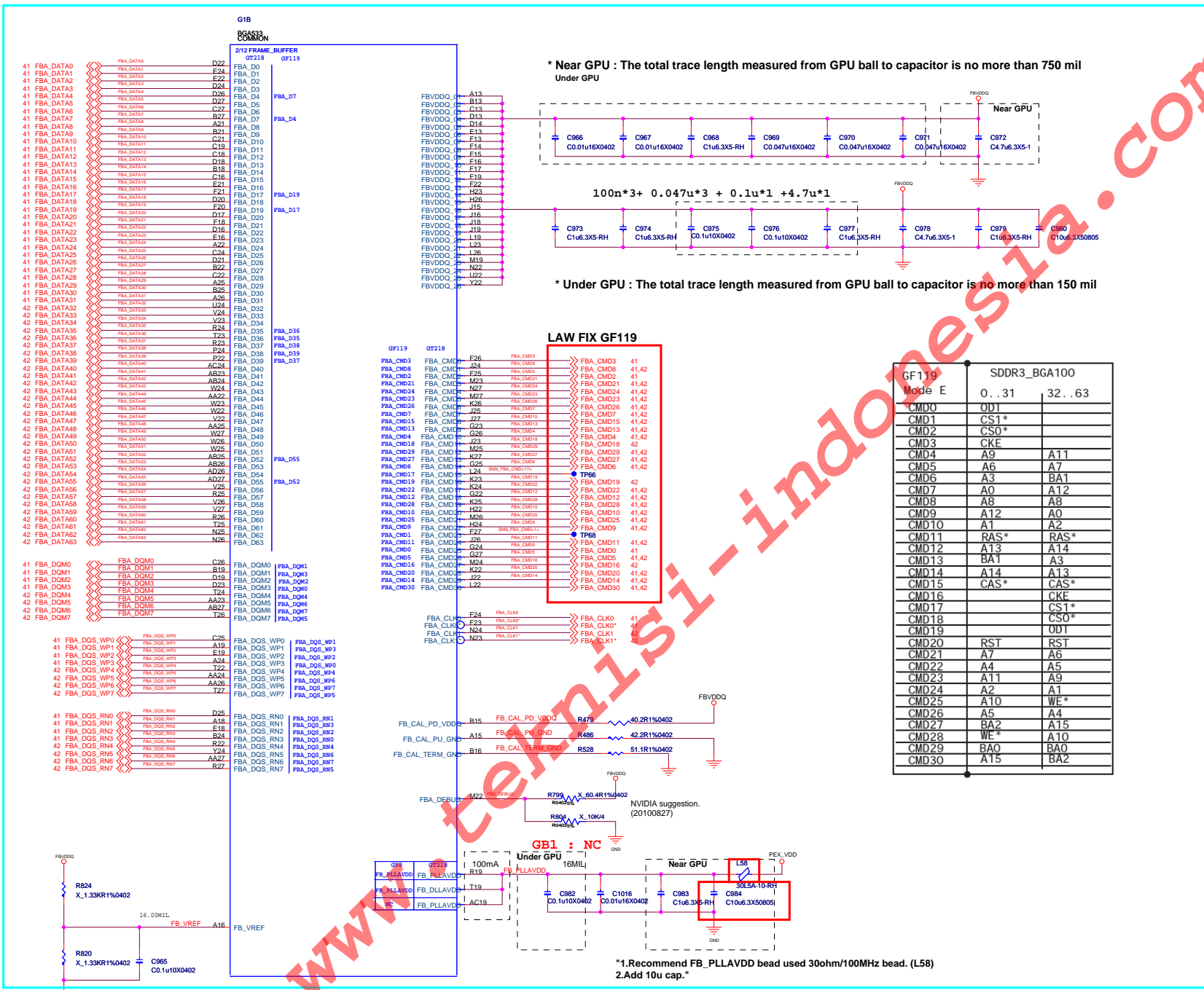
- * Near GPU : The total trace length measured from GPU ball to capacitor is no more than 750 mil
- * Under GPU : The total trace length measured from GPU ball to capacitor is no more than 150 mil



MICRO-STAR INT'L CO.,LTD

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* Near GPU : The total trace length measured from GPU ball to capacitor is no more than 750 mil
Under GPU

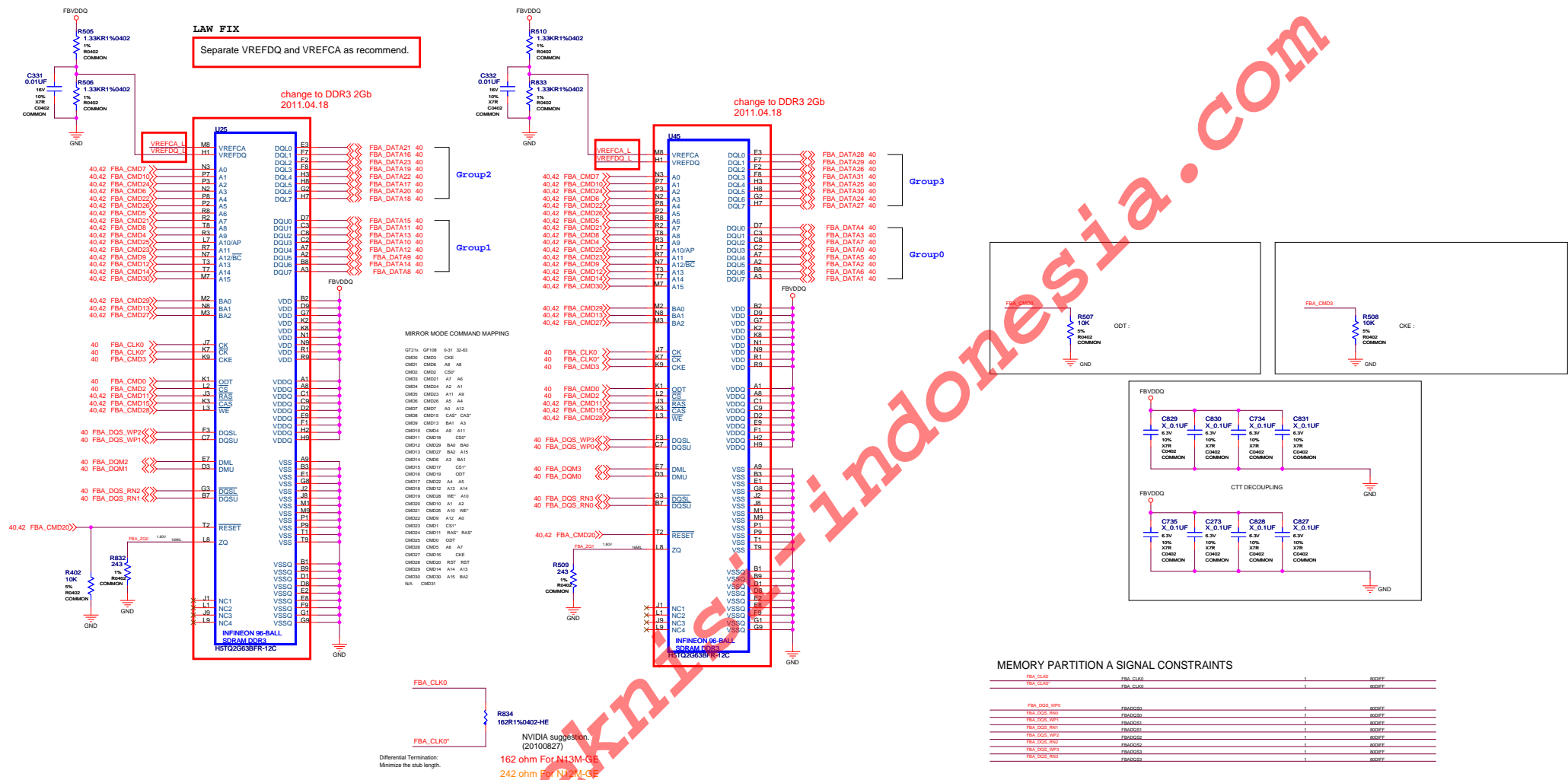
* Under GPU : The total trace length measured from GPU ball to capacitor is no more than 150 mil

LAW FIX GF119

GF119		SDDR3_BGA100	
Mode E	0..31	32..63	
CMD0	ODT		
CMD1	CS1*		
CMD2	CS0*		
CMD3	CKE		
CMD4	A9	A11	
CMD5	A6	A7	
CMD6	A3	BA1	
CMD7	A0	A12	
CMD8	A8	AB	
CMD9	A12	A0	
CMD10	A1	A2	
CMD11	RAS*	RAS*	
CMD12	A13	A14	
CMD13	BA1	A3	
CMD14	A14	A13	
CMD15	CAS*	CAS*	
CMD16		CKE	
CMD17		CS1*	
CMD18		CS0*	
CMD19	ODT		
CMD20	RST	RST	
CMD21	A7	A6	
CMD22	A4	A5	
CMD23	A11	A9	
CMD24	A2	A1	
CMD25	A10	WE*	
CMD26	A5	A4	
CMD27	BA2	A15	
CMD28	WE	A10	
CMD29	BA0	BA0	
CMD30	A15	BA2	

"1.Recommend FB_PLLAVDD bead used 30ohm/100MHz bead. (L58)
2.Add 10u cap."

4. MEMORY PARTITION A LOWER 32 BITS



MEMORY PARTITION A SIGNAL CONSTRAINTS

FBA_C420	FBA_C420	1	NOEF
FBA_C427	FBA_C427	1	NOEF
FBA_C505_WF0	FBA_C505	1	NOEF
FBA_C505_WF0	FBA_C505	1	NOEF
FBA_C505_WF1	FBA_C505	1	NOEF
FBA_C505_WF1	FBA_C505	1	NOEF
FBA_C505_WF2	FBA_C505	1	NOEF
FBA_C505_WF2	FBA_C505	1	NOEF
FBA_C505_WF3	FBA_C505	1	NOEF
FBA_C505_WF3	FBA_C505	1	NOEF
FBA_C505_WF4	FBA_C505	1	NOEF
FBA_C505_WF4	FBA_C505	1	NOEF



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5. MEMORY PARTITION A UPPER 32 BITS

LAW FIX

Separate VREFDQ and VREFCA as recommend.

change to DDR3 2Gb
2011.04.18

change to DDR3 2Gb
2011.04.18

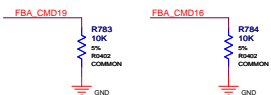
MIRROR MODE COMMAND MAPPING

0710	0710	031	32A3
CM00	CM00	CM00	CM00
CM01	CM01	CM01	CM01
CM02	CM02	CM02	CM02
CM03	CM03	CM03	CM03
CM04	CM04	CM04	CM04
CM05	CM05	CM05	CM05
CM06	CM06	CM06	CM06
CM07	CM07	CM07	CM07
CM08	CM08	CM08	CM08
CM09	CM09	CM09	CM09
CM10	CM10	CM10	CM10
CM11	CM11	CM11	CM11
CM12	CM12	CM12	CM12
CM13	CM13	CM13	CM13
CM14	CM14	CM14	CM14
CM15	CM15	CM15	CM15
CM16	CM16	CM16	CM16
CM17	CM17	CM17	CM17
CM18	CM18	CM18	CM18
CM19	CM19	CM19	CM19
CM20	CM20	CM20	CM20
CM21	CM21	CM21	CM21
CM22	CM22	CM22	CM22
CM23	CM23	CM23	CM23
CM24	CM24	CM24	CM24
CM25	CM25	CM25	CM25
CM26	CM26	CM26	CM26
CM27	CM27	CM27	CM27
CM28	CM28	CM28	CM28
CM29	CM29	CM29	CM29
CM30	CM30	CM30	CM30
CM31	CM31	CM31	CM31
CM32	CM32	CM32	CM32
CM33	CM33	CM33	CM33
CM34	CM34	CM34	CM34
CM35	CM35	CM35	CM35
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CM37	CM37	CM37	CM37
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CM39	CM39	CM39	CM39
CM40	CM40	CM40	CM40
CM41	CM41	CM41	CM41
CM42	CM42	CM42	CM42
CM43	CM43	CM43	CM43
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CM46	CM46	CM46	CM46
CM47	CM47	CM47	CM47
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CM97	CM97	CM97	CM97
CM98	CM98	CM98	CM98
CM99	CM99	CM99	CM99
CM100	CM100	CM100	CM100

FBA_DQS_WP4	FBA_DQS_WP4	1	SOFF
FBA_DQS_WP5	FBA_DQS_WP5	1	SOFF
FBA_DQS_WP6	FBA_DQS_WP6	1	SOFF
FBA_DQS_WP7	FBA_DQS_WP7	1	SOFF
FBA_DQS_WP8	FBA_DQS_WP8	1	SOFF
FBA_DQS_WP9	FBA_DQS_WP9	1	SOFF
FBA_DQS_WP10	FBA_DQS_WP10	1	SOFF
FBA_DQS_WP11	FBA_DQS_WP11	1	SOFF
FBA_DQS_WP12	FBA_DQS_WP12	1	SOFF
FBA_DQS_WP13	FBA_DQS_WP13	1	SOFF
FBA_DQS_WP14	FBA_DQS_WP14	1	SOFF
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FBA_DQS_WP49	FBA_DQS_WP49	1	SOFF
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FBA_DQS_WP95	FBA_DQS_WP95	1	SOFF
FBA_DQS_WP96	FBA_DQS_WP96	1	SOFF
FBA_DQS_WP97	FBA_DQS_WP97	1	SOFF
FBA_DQS_WP98	FBA_DQS_WP98	1	SOFF
FBA_DQS_WP99	FBA_DQS_WP99	1	SOFF
FBA_DQS_WP100	FBA_DQS_WP100	1	SOFF

Differential Termination:
Minimize the stub length.

162 ohm For N13M-GE
242 ohm For N12M-GE



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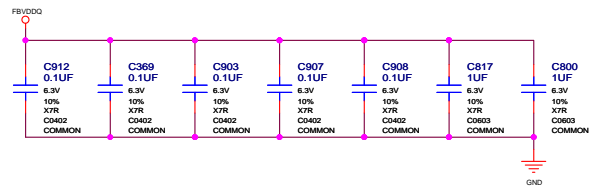
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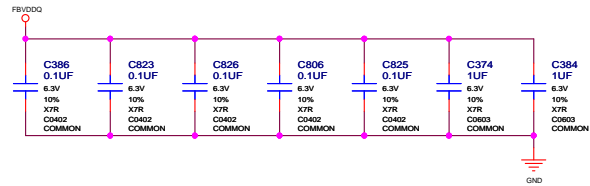
8. MEMORY DECOUPLING CAPS

Cost down won't recommend.

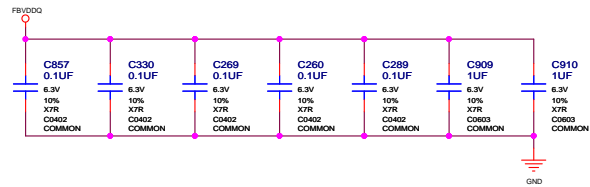
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 0-15



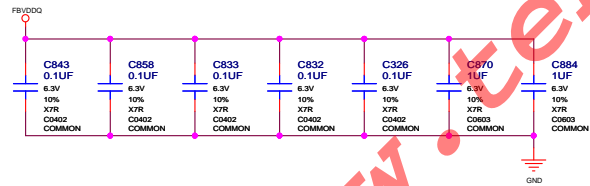
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 16-31



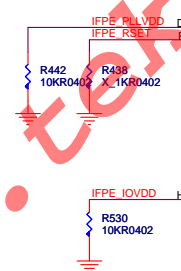
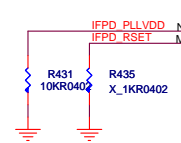
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 32-47



DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 48-63



PCB layout showing power planes, decoupling capacitors, and component footprints for a BGA533 processor. The layout includes a top power plane with decoupling capacitors (C753, C791, C745, C747, C985, C749) and a bottom power plane with decoupling capacitors (R431, R435, R442, R438, R530). Component footprints for BGA533, GT218, and GT128 are shown. A large red watermark 'www.torisiindonesia.com' is overlaid on the image.

[illegible]

B014533 COMMON		NOT USED	
8/12 IFPD			
IFPD_PLLVDD IFPD_RSET			
D <			

NOT USED

G1D
80A5333
COMMON

8/12 IFPE

GT128	G98
IFPE_FLVDD	DACB_VDD
IFPE_RSET	DACB_RSET

G98		GT218	
DACB		DV/HVDDMI	DP
DACB_VREF	I2CY_SDA		IFPE_AUX
DACB_RED	I2CY_SCL		IFPE_AUX
DACB_GREEN	TXC		IFPE_LC
DACB_BLUE	TXC		IFPE_LC
HDA_SYNC	TXD0		IFPE_LC
HDA_SDO	TXD0		IFPE_LC
HDA_BCLK	TXD1		IFPE_LC
HDA_SDI	TXD1		IFPE_LC
HDA_RST_N	TXD2		IFPE_LC
DACB_CSNG	TXD2		IFPE_LC

E

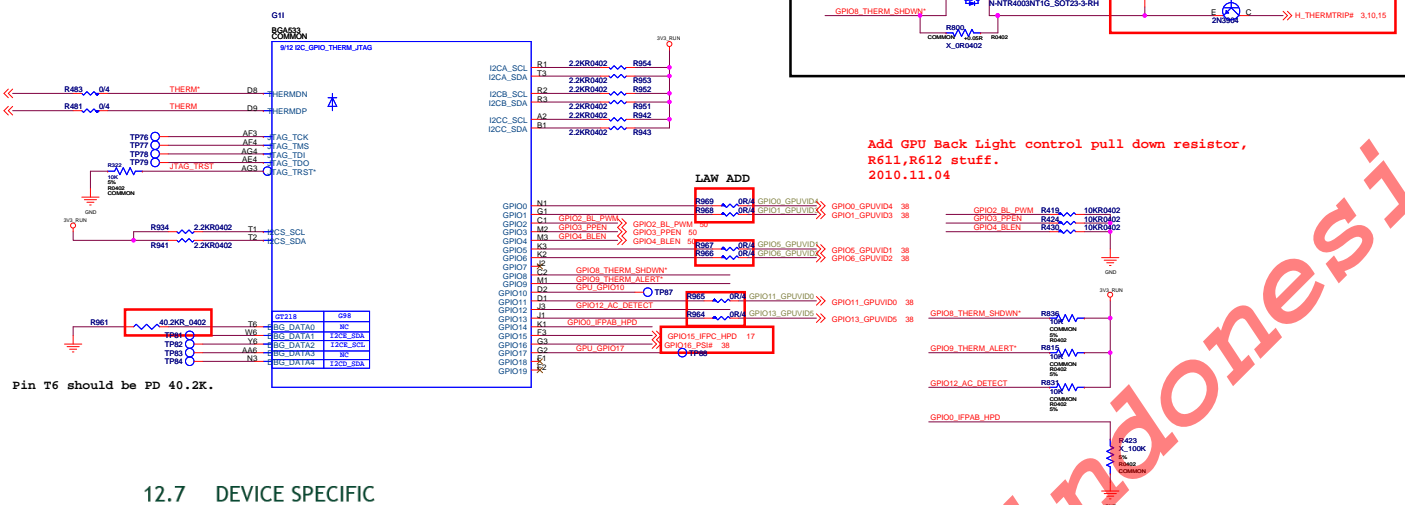
IFPE_I0VDD0

LAW ADD 20111121

DEL EDP



12. GPIO, JTAG, TEMP SENSOR, Info ROM



12.7 DEVICE SPECIFIC

Table 96 outlines the default functions of the GPIO signals in notebook applications. These functions may be altered with the approval of NVIDIA's software design support team.

Table 96. GPIO Description

GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	0	GPU Core VDD VID4
GPIO1	GPU_VID3	0	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	0	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC or PSI	0	Panel Power Enable or Phase Shedding
GPIO4	LCD_BLEN	0	Panel Backlight Enable
GPIO5	GPU_VID1	0	GPU Core VDD VID1
GPIO6	GPU_VID2	0	GPU Core VDD VID2
GPIO7	3D Vision	0	3D Vision Lift/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	0	Memory VREF Control
GPIO11	GPU_VID0	0	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input
GPIO13	GPU_VID5	0	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	PSI or MEM_VDD_CTL	0	Phase Shedding or Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

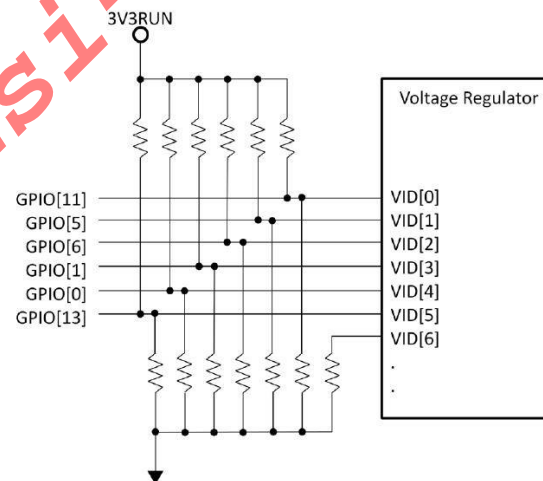
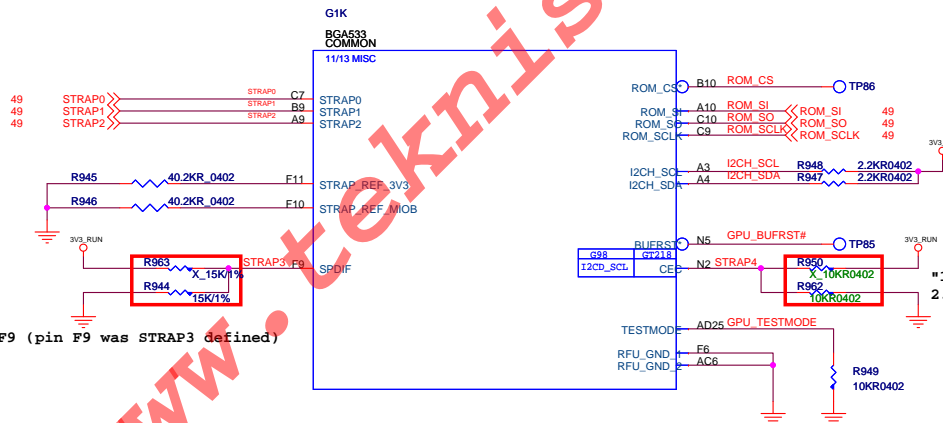
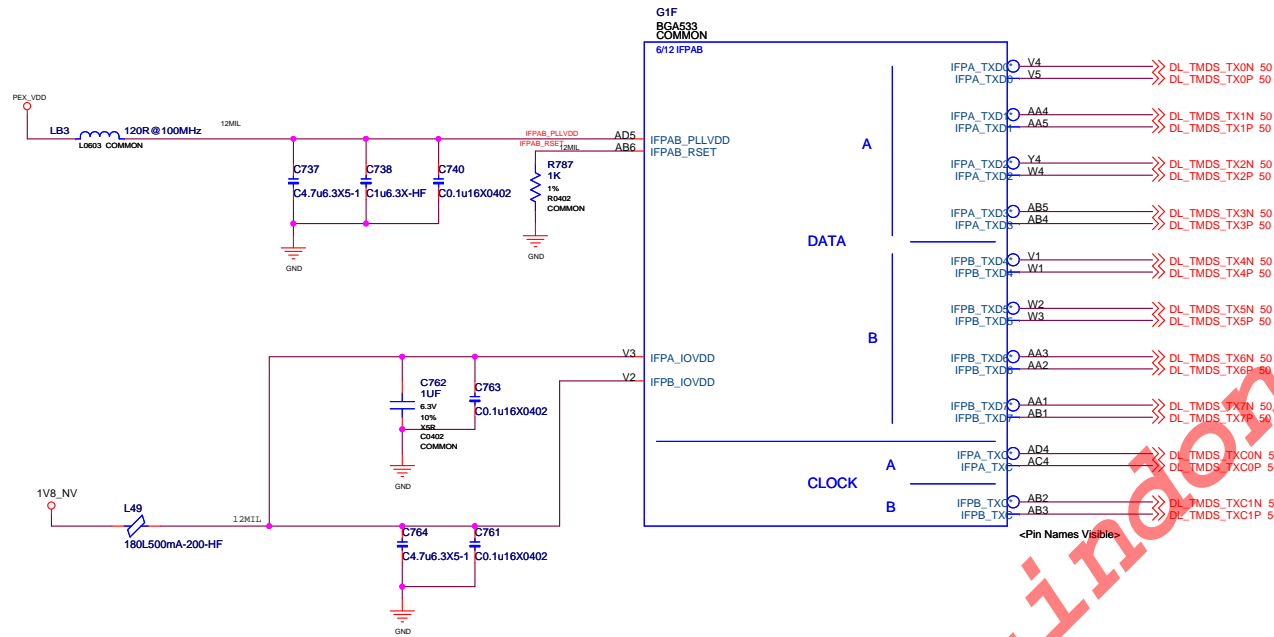


Figure 1. GPIO and VID Connection

13. LVDS, VBIOS

LVDS



"1.Add PU and PD circuit at pin F9 (pin F9 was STRAP3 defined)
2.PD 15K at pin F9(0010)"

"1.Add PU and PD circuit at pin N2 (pin N2 was STRAP4 defined)
2.PD 10K at pin N2 (0001)"

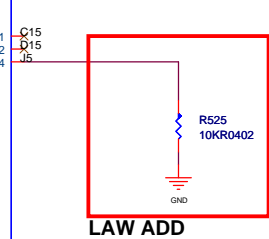
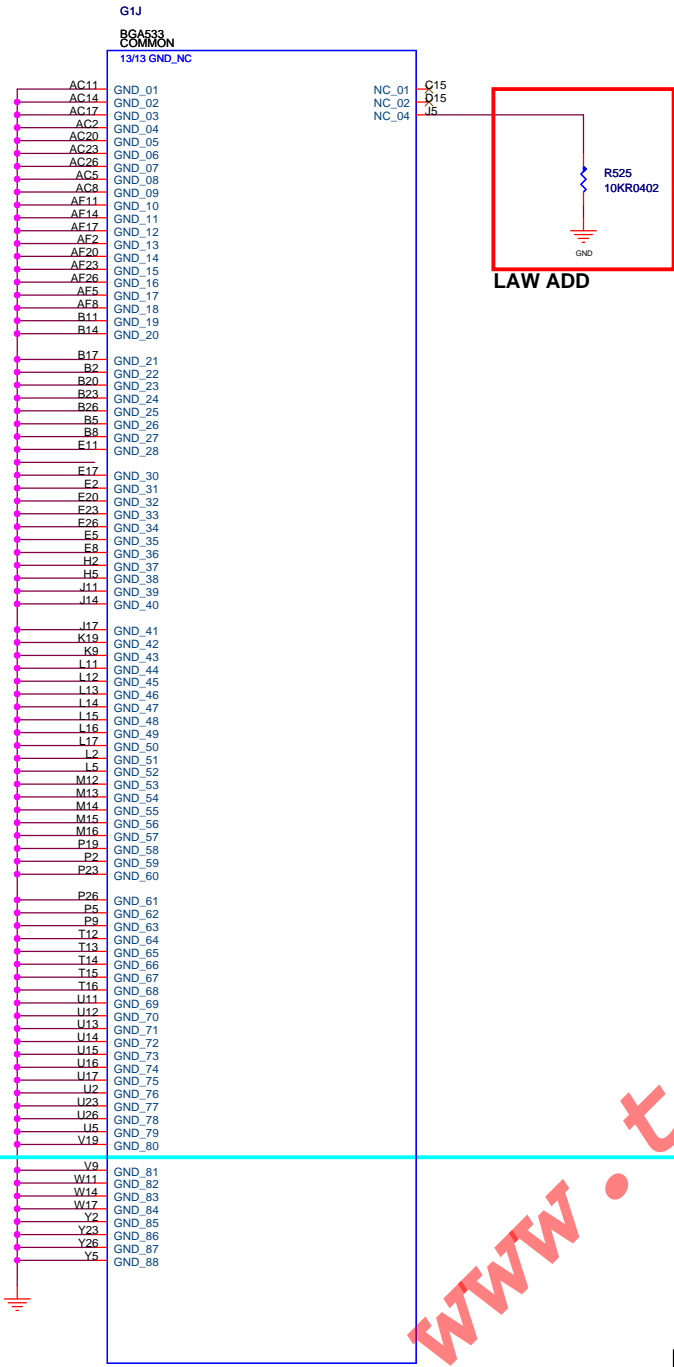


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14. MIOA, MIOB, GPU VDD/DCPLNG/GND



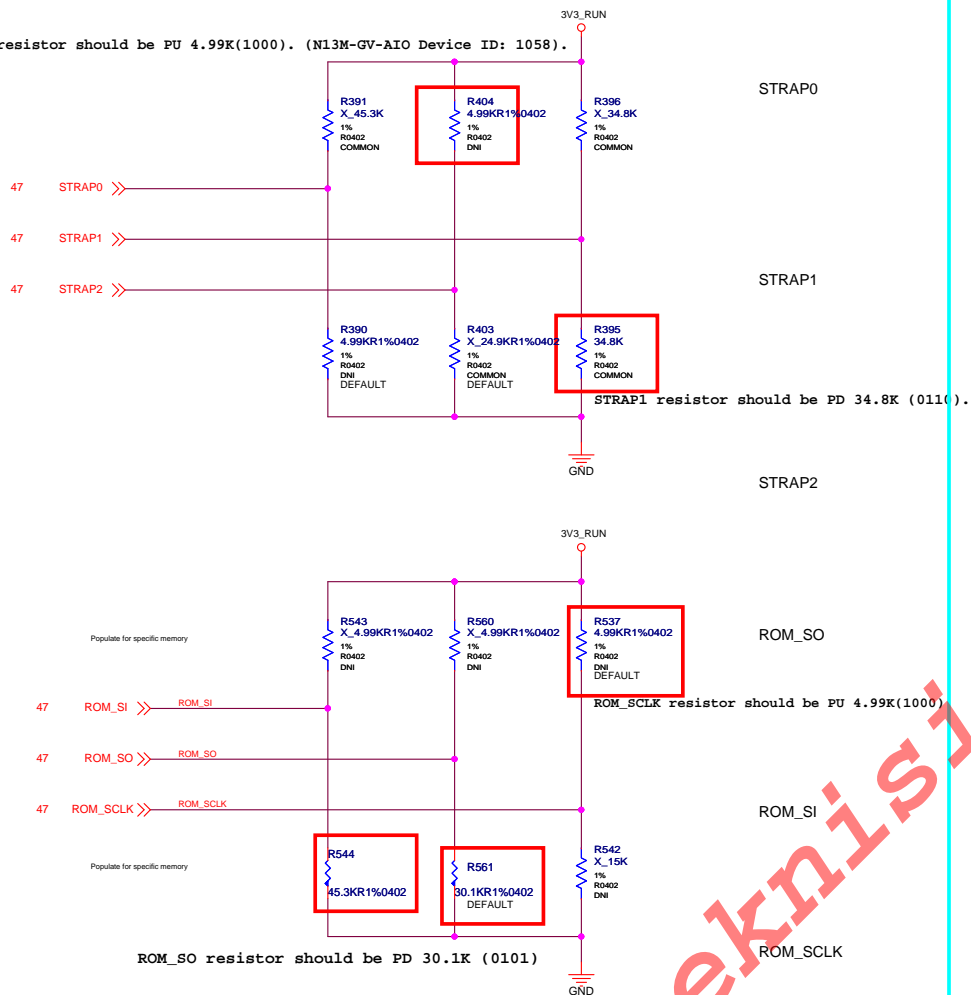
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17. STRAPS, MOUNTING HOLES

STRAP0 was defined to select LVDS panel, if EDID was saved through VBIOS,
PD 5K = 0000 (It means EDID save table 0)



Manufacturer	Part Number	Die	Resistor Value
SAMSUNG	M12-K4W2G35-S02	B-Die	R544 45k PD (R11-4532T12-W08) 45.3k
HYNIX	M12-5TQ2GE5-H23	D-die	R544 35k PD (R11-3482T12-W08) 34.8k

USER_BIT0

USER_BIT1

USER_BIT2

USER_BIT3

Default All SKU(s):

0xF = 45K PU

LVDS Panel EDID Mode

3GIO_PADCFG_LUT_ADR0

3GIO_PADCFG_LUT_ADR1

3GIO_PADCFG_LUT_ADR2

3GIO_PADCFG_LUT_ADR3

Set at HW reset by the PEX_PADCFG Circuit

0x0: Desktop default (normal swing) - 5k PD

0x1: Mobile default (low swing) - 10k PD

PCI_DEVID_0

PCI_DEVID_1

PCI_DEVID_2

PCI_DEVID_3

PCDEVID_3:0] Definitions (Note Actual DEVID set also depends on PCI_DEVID_4)

GT218

GT216

GF108

1000 5K PU GT218-700

0100 25K PD GT218-730

1000 5K PU GT216-600

0100 25K PD GT216-630

1100 25K PU GT216-640

1100 25K PU GT216-950

0000 5K PD GF108-630

VGA_DEVICE 0: 3D DEVICE

1: VGA DEVICE

Set at HW reset by the Device Detect Circuit

SMB_ALT_ADDR 0: Thermal Sensor ADR = 0x9E

0x1 = 10K PD

FB_0_BAR_SIZE 0: Default

XCLK_417 0: Default

RAM_CFG[3:0] Definitions

GT215/6

RAM_CFG_0 GF108 64Mx16

0000 5K PD Reserved

0001 10K PD Reserved

0010 15K PD HYNIX

0011 20K PD SAMSUNG

RAM_CFG_1

RAM_CFG_2 GT108 128Mx16

0100 25k PD Reserved

0101 30k PD Reserved

0110 35k PD HYNIX

0111 45k PD SAMSUNG

0001 Reserved

0001 64Mx16 128-bit 10K PD Qimonda

0010 64Mx16 128-bit 15K PD Hynix

0011 64Mx16 128-bit 20K PD Samsung

0100 Reserved

0101 32Mx16 128-bit 30K PD Qimonda

0110 32Mx16 128-bit 35K PD Hynix

0111 32Mx16 128-bit 45K PD Samsung

1001 Reserved

1001 64Mx16 64-bit 10K PU Qimonda

1010 64Mx16 64-bit 15K PU Hynix

1011 64Mx16 64-bit 20K PU Samsung

1100 Reserved

1101 128Mx16 64-bit 30K PU Qimonda

1110 128Mx16 64-bit 35K PU Hynix

1111 128Mx16 64-bit 45K PU Samsung

* 32Mx16 MAY BE 64Mx16 run at 1/2 density

PEX_PLL_EN_TERM100 0: DISABLED

SLOT_CLK_CONFIG 1: GPU and MCH COMMON REFCLK

0x6 = 35K PD PCDEVID_EXT=0

SUB_VENDOR 1: VBIOS ROM IS PRESENT

0xE = 35K PU PCDEVID_EXT=1

PCI_DEVID_EXT 0: PCDEVID[4] = 0 or 1 (SKU Specific)

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111



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Size Custom

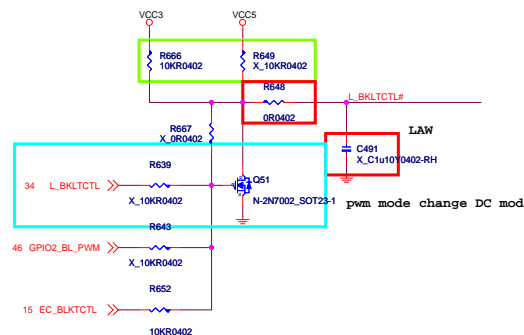
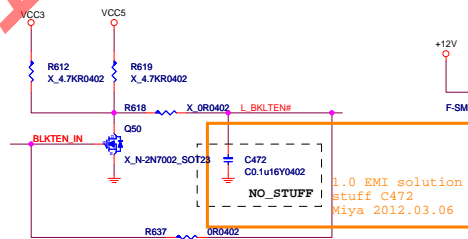
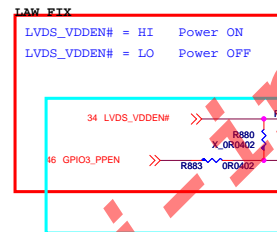
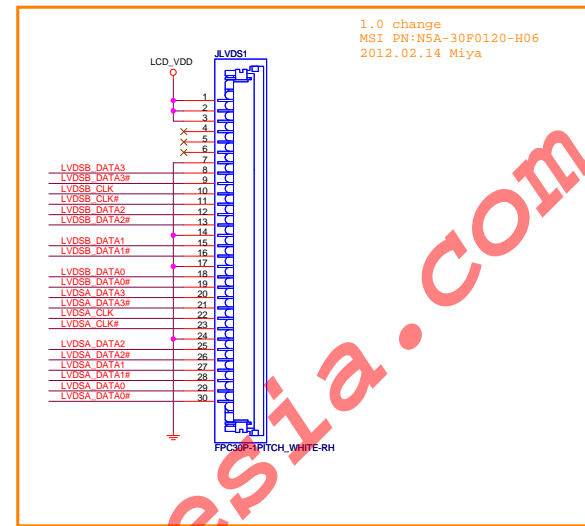
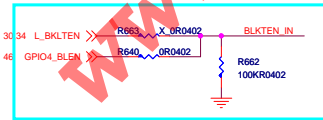
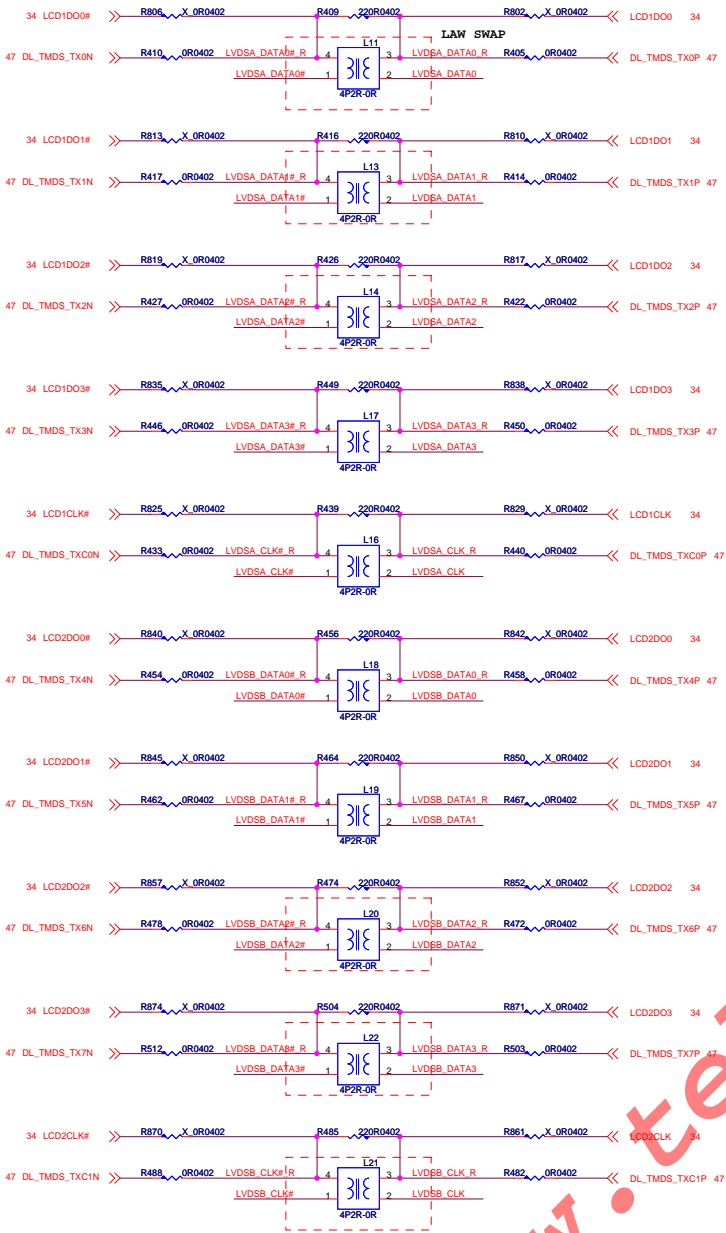
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GPU STRAPS

Rev 10

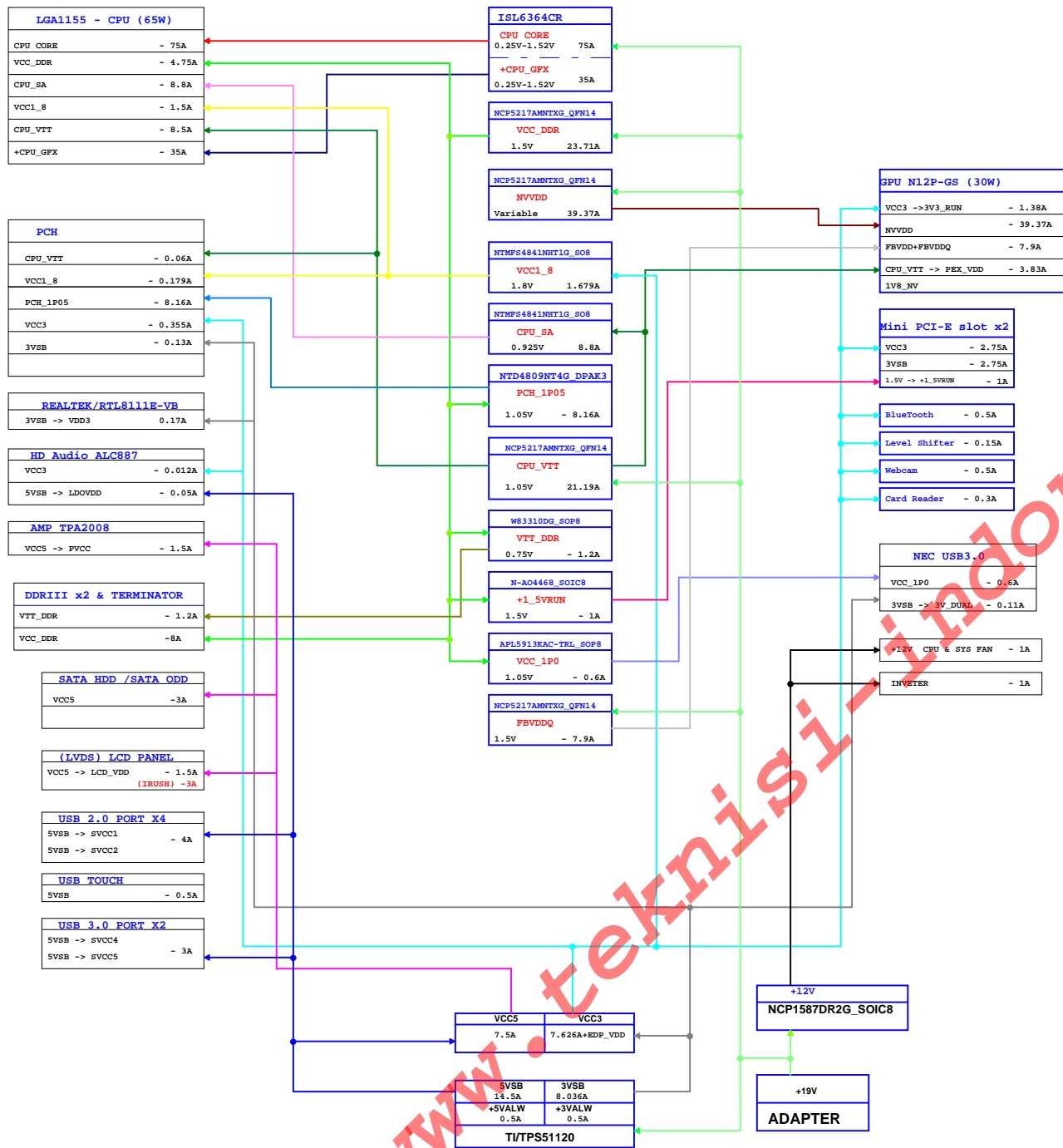
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MODE	R648	C491
PWM	0 ohm	unstuff
DC	4.7k ohm	stuff

P10 FIX PCH_GPIO68



P3 R705 UNSTUFF
P11 Add CLR_CMD switch
P11 C10B0 unstuff
P20 1.0 STUFF AMP TA2008
P23 add FAN protect circuit
P28 power cost down
P29 (+CPU_FFX) GPU SED unstuff , cost down
P30 modify switch button name
P33 USB5 & USB9 net exchange
P34 R501 UNSTUFF
P35 USB5 & USB9 net exchange
P35 TV TUNER PULL HIGH VCC3 (R144)
P35 modify net/PCTE_MINT_PDN5 /PCTE_MINT_RXP5
P37 Add R864 --->TOUT_FOM 20+ SED [1] (USB 2.0)
P50 change LOTS connector PW/MSA-30P5120-R06
P4 stuff C96
P26 RMI solution stuff R697 / C577
P27 RMI solution stuff R6774 / C674
P38 RMI solution stuff P618 / P614
P35 Add J1 JAMPER (default VCC3)
P35 AVerMedia TV card stuff R546 (VCC3)
P29 Power solution Del C194 /C197 /C191 /C207 , stuff RCT2 / RCT3
P39 Del R5C7 /R5C8 /R5C9
P39 PRC1 / PRC2 /PRC5 (540u/2.5V) SMT change DIP
P11 V1 DIP chage SMT / C221/C222 change 18P
P36 Q41 /Q77 change type
P19 Add C759 for RMI solution
P17 RMI solution stuff R583/R557/R558/R587 change to 220 ohm
P50 RMI solution stuff C472
P36 RMI solution stuff C516 /C518
P14 R145 change to 1K ohm
P14 22" change RXP MCI PW/BDP-034601C-047
P14 WCC change new RCI PU
High S16w Q13/Q16/Q20
Low Side Q11/Q12/Q14/Q15/Q17/Q18

P21 cost down unstuff system fan connector

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